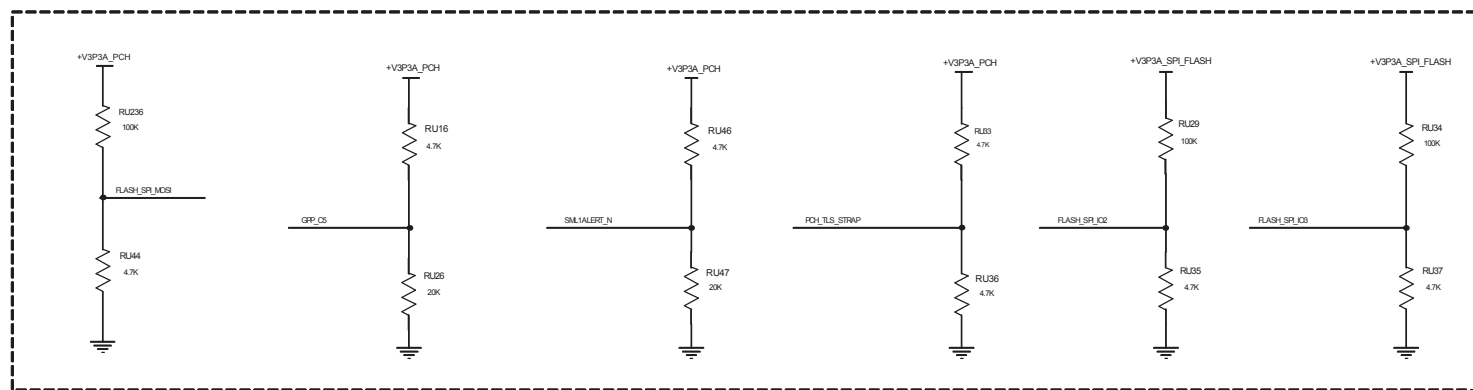
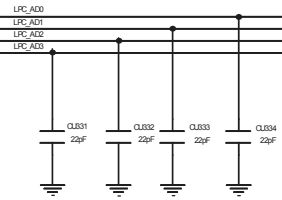
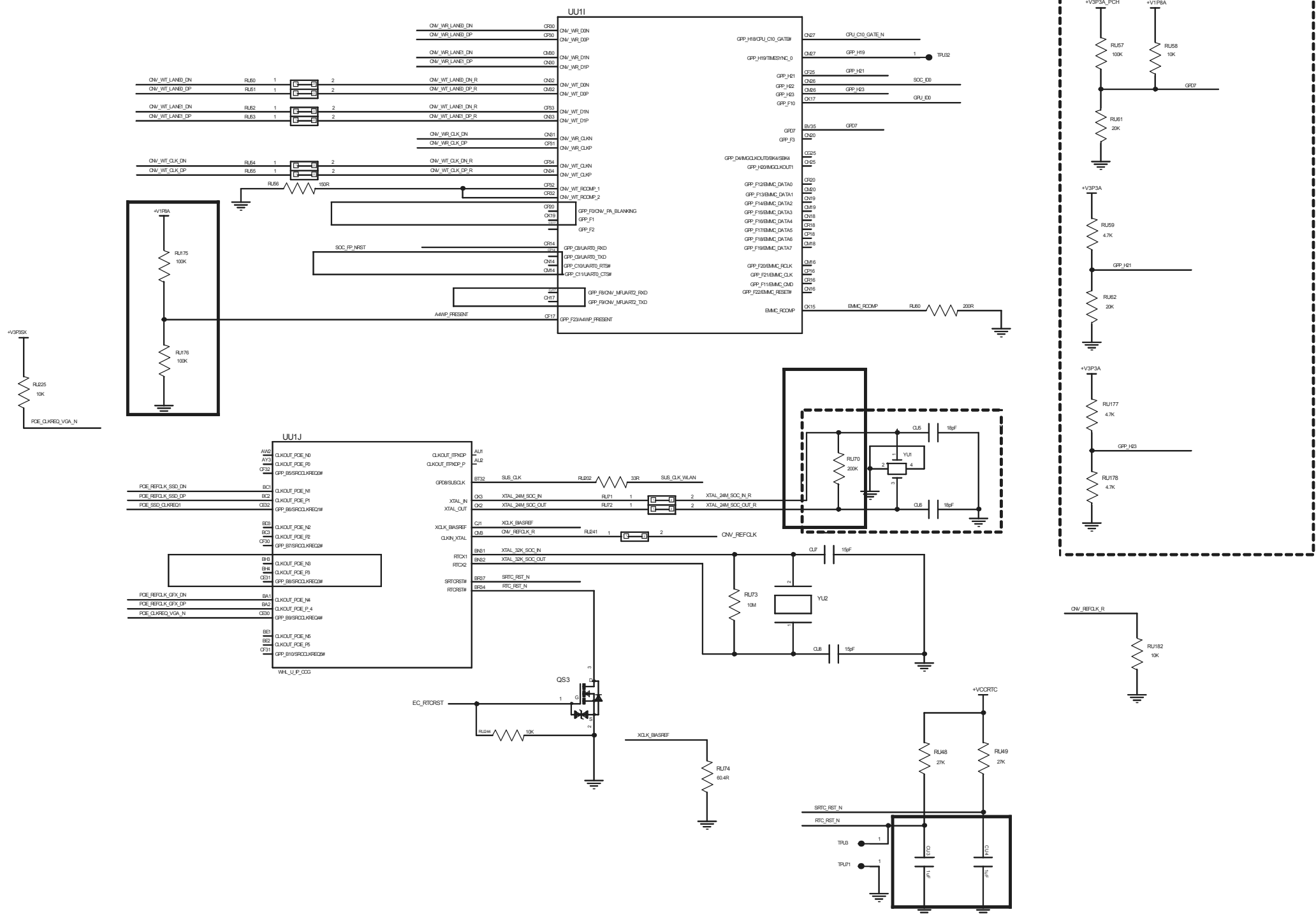
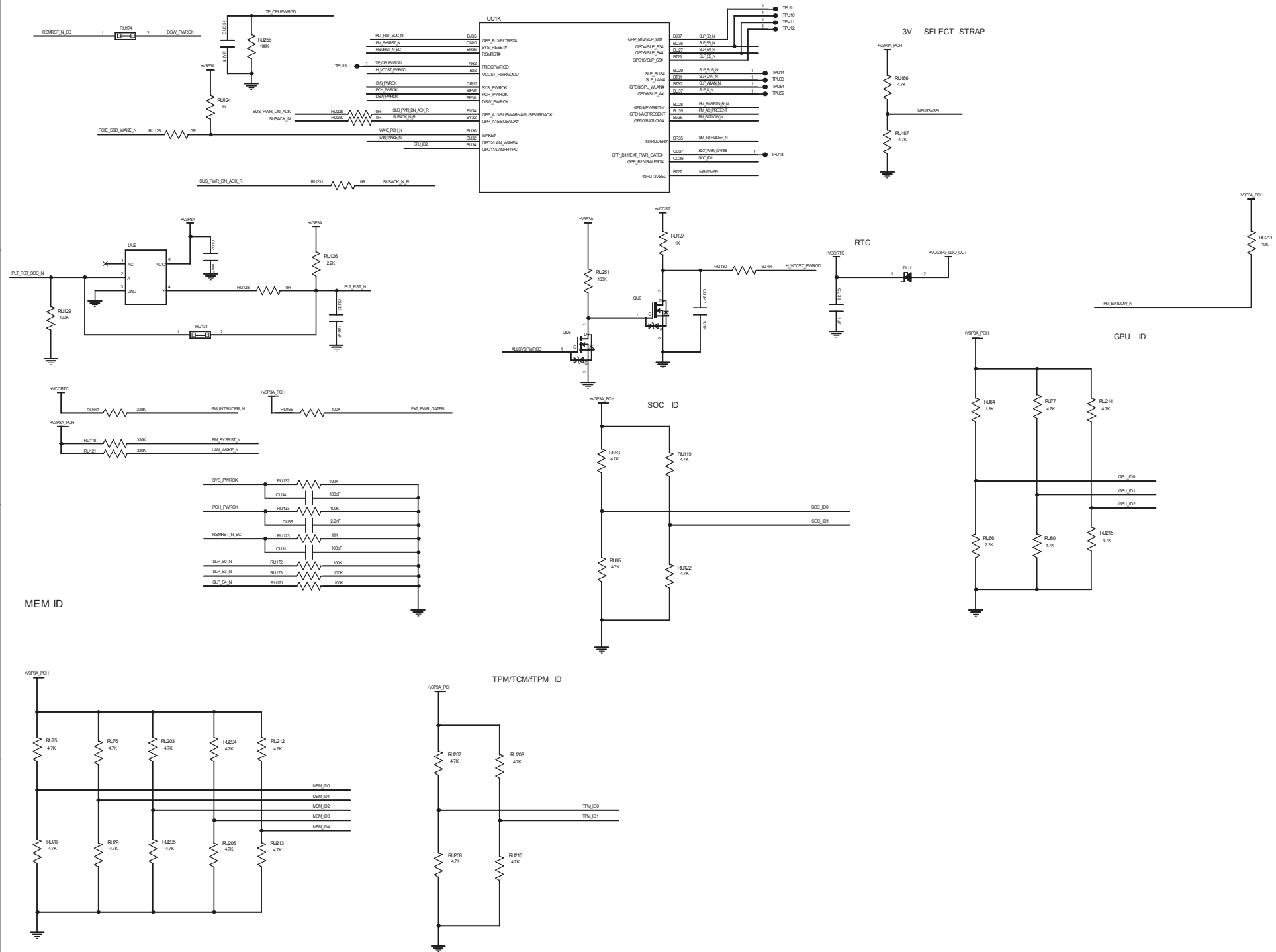
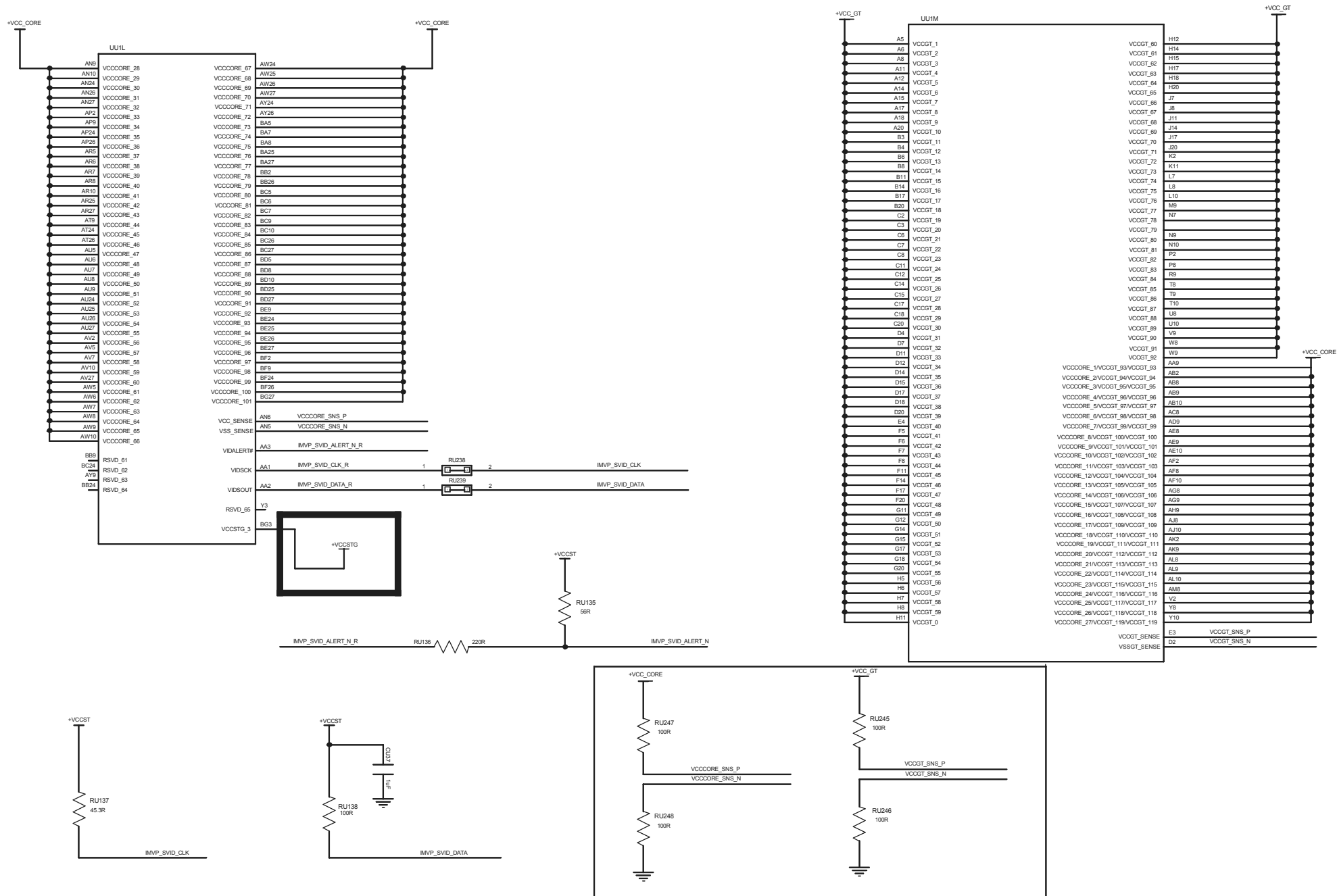


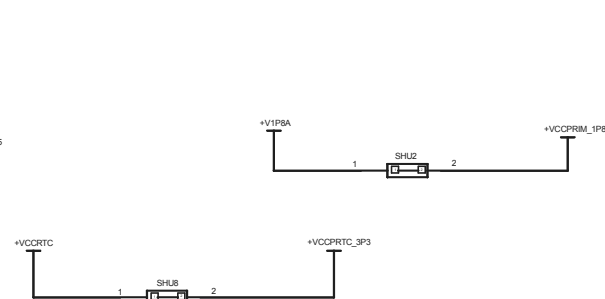
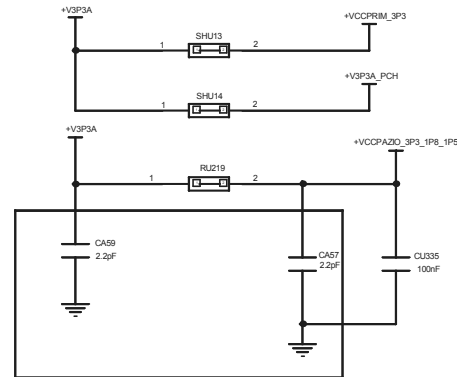
WHL_U_IP_CCG

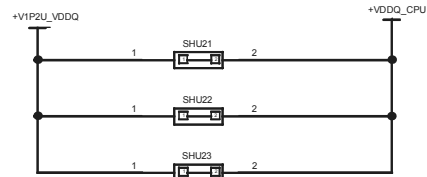








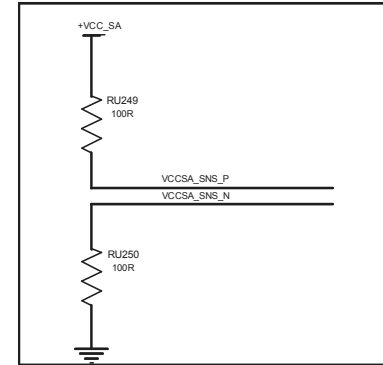
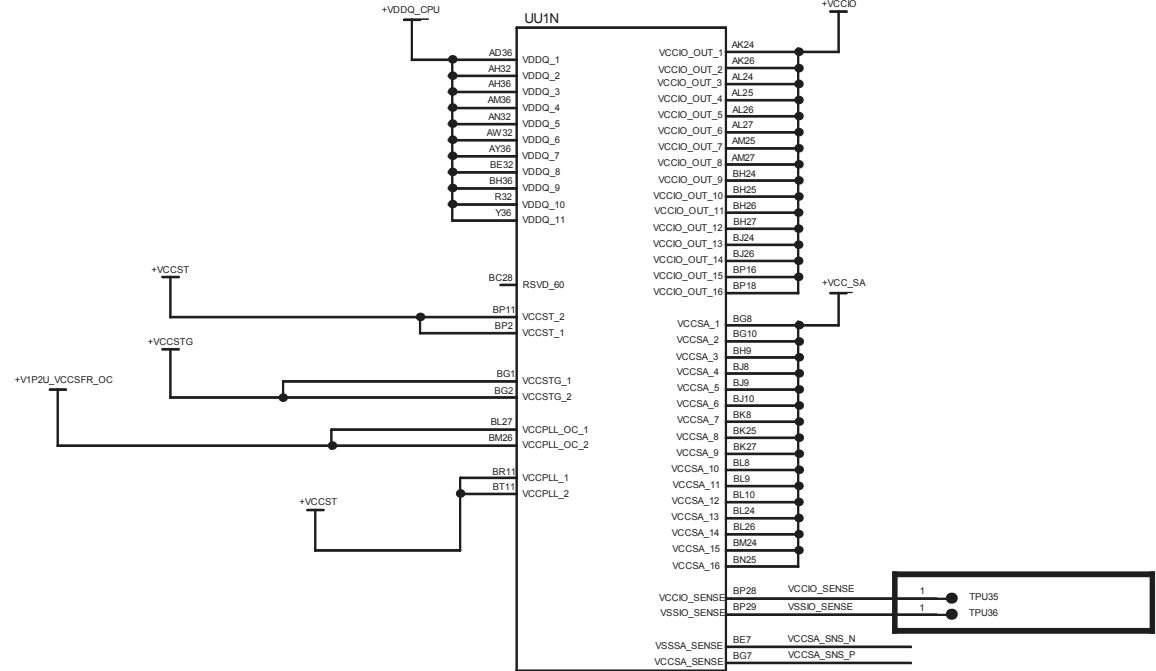


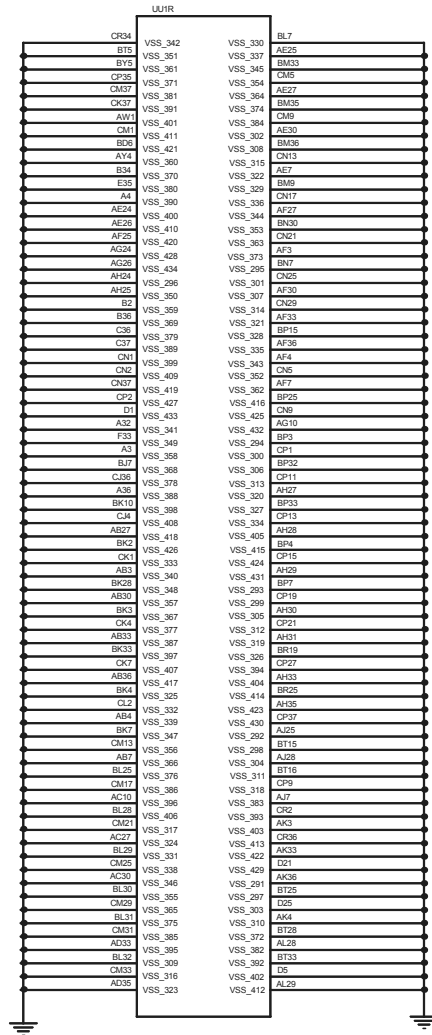


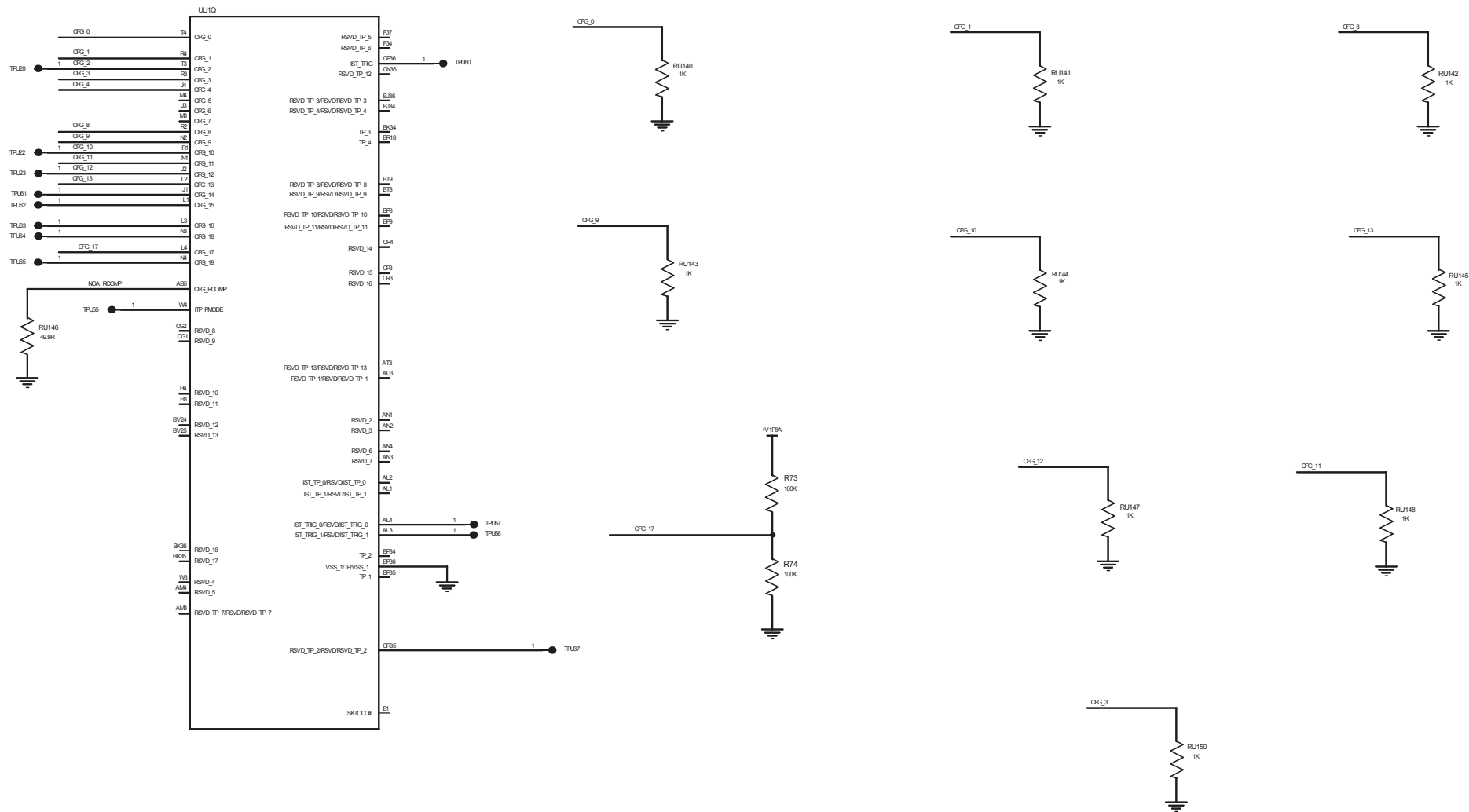
UU10

K12	RSVD_25VCC_OPC_1/RSVD_25	AA24	RSVD_38VCCOPIO_1/RSVD_38
K14	RSVD_26VCC_OPC_2/RSVD_26	AA26	RSVD_40VCCOPIO_2/RSVD_40
K15	RSVD_27VCC_OPC_3/RSVD_27	AB25	RSVD_41VCCOPIO_3/RSVD_41
K17	RSVD_28VCC_OPC_4/RSVD_28	AC24	RSVD_42VCCOPIO_4/RSVD_42
K18	RSVD_29VCC_OPC_5/RSVD_29	AC25	RSVD_43VCCOPIO_5/RSVD_43
K20	RSVD_30VCC_OPC_6/RSVD_30	AC26	RSVD_44VCCOPIO_6/RSVD_44
L28	RSVD_31VCC_OPC_7/RSVD_31	AD24	RSVD_45VCCOPIO_7/RSVD_45
M24	RSVD_32VCC_OPC_8/RSVD_32	AD26	RSVD_46VCCOPIO_8/RSVD_46
M26	RSVD_33VCC_OPC_9/RSVD_33	V25	RSVD_19VCCOPIO_SENSE/RSVD_19
P24	RSVD_34VCC_OPC_10/RSVD_34	T25	RSVD_20VSSOPIO_SENSE/RSVD_20
P26	RSVD_35VCC_OPC_11/RSVD_35	RSVD_56	RSVD_56
R24	RSVD_36VCC_OPC_12/RSVD_36	RSVD_57	RSVD_57
R25	RSVD_37VCC_OPC_13/RSVD_37	D34	RSVD_58/OPCE_RCOMP/RSVD_58
R26	RSVD_38VCC_OPC_14/RSVD_38	N5	
V24	RSVD_21VCC_OPC_1P8_3/RSVD_21		
W25	RSVD_22VCC_OPC_1P8_4/RSVD_22		
Y24	RSVD_23VCC_OPC_1P8_1/RSVD_23		
Y25	RSVD_24VCC_OPC_1P8_2/RSVD_24		
G2	RSVD_47		
G1	RSVD_48		
C34	RSVD_49VSS_435/RSVD_49		
G3	RSVD_50VSS_436/RSVD_50		
G4	RSVD_51VSS_437/RSVD_51		
A34	RSVD_52/RSVD_TP/RSVD_52		
B35	RSVD_53/RSVD_TP/RSVD_53		
AJ27	RSVD_54/MSM/RSVD_54		
AJ28	RSVD_55/Z/M/RSVD_55		
L5	RSVD_56/OPCE_RCOMP/RSVD_56		

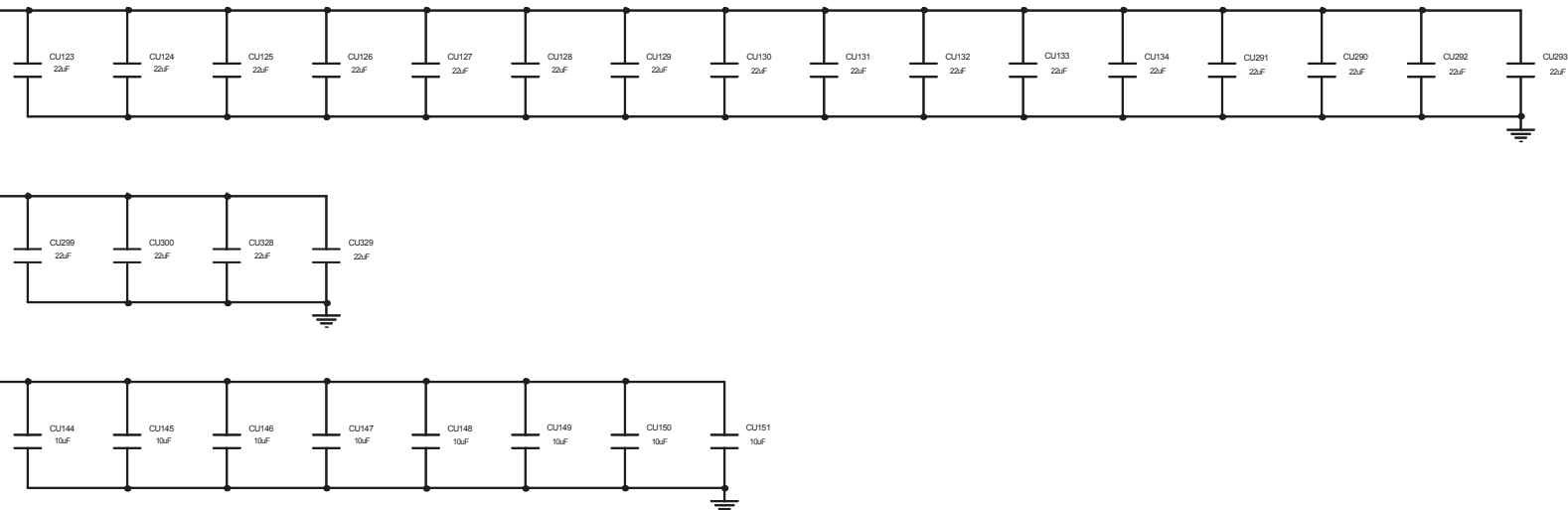
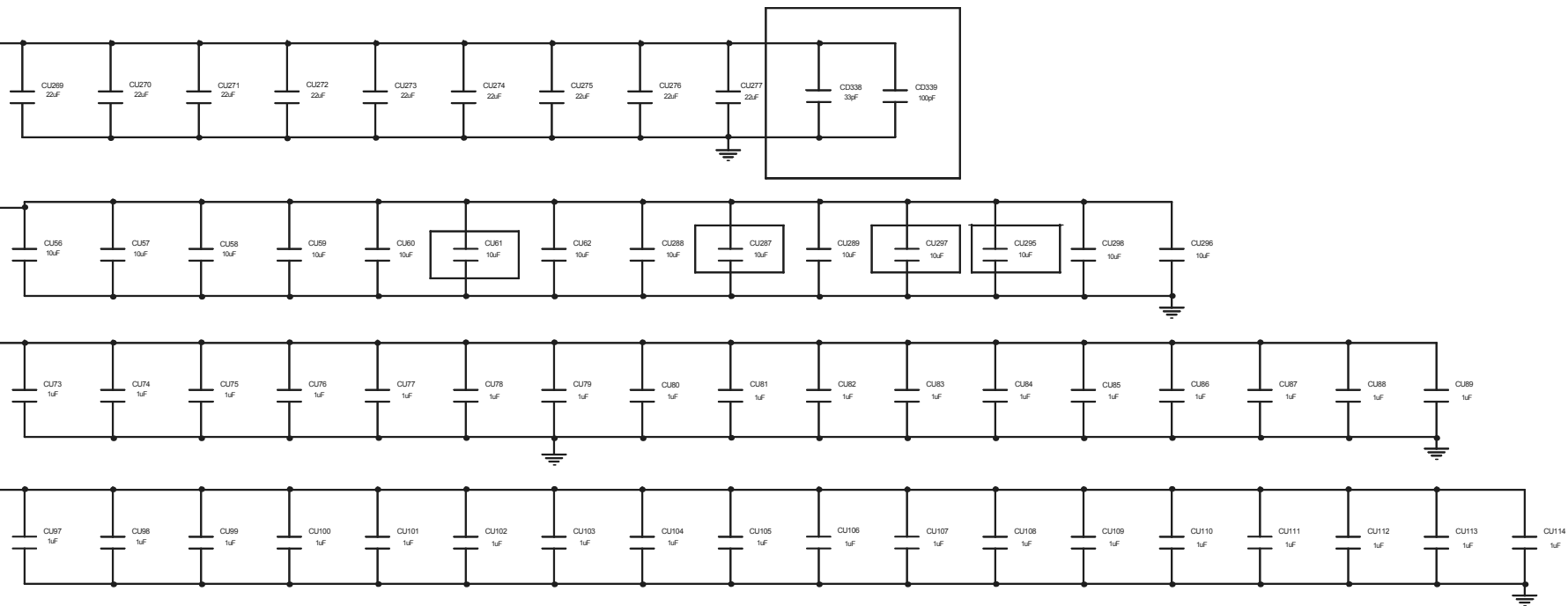
UU1N

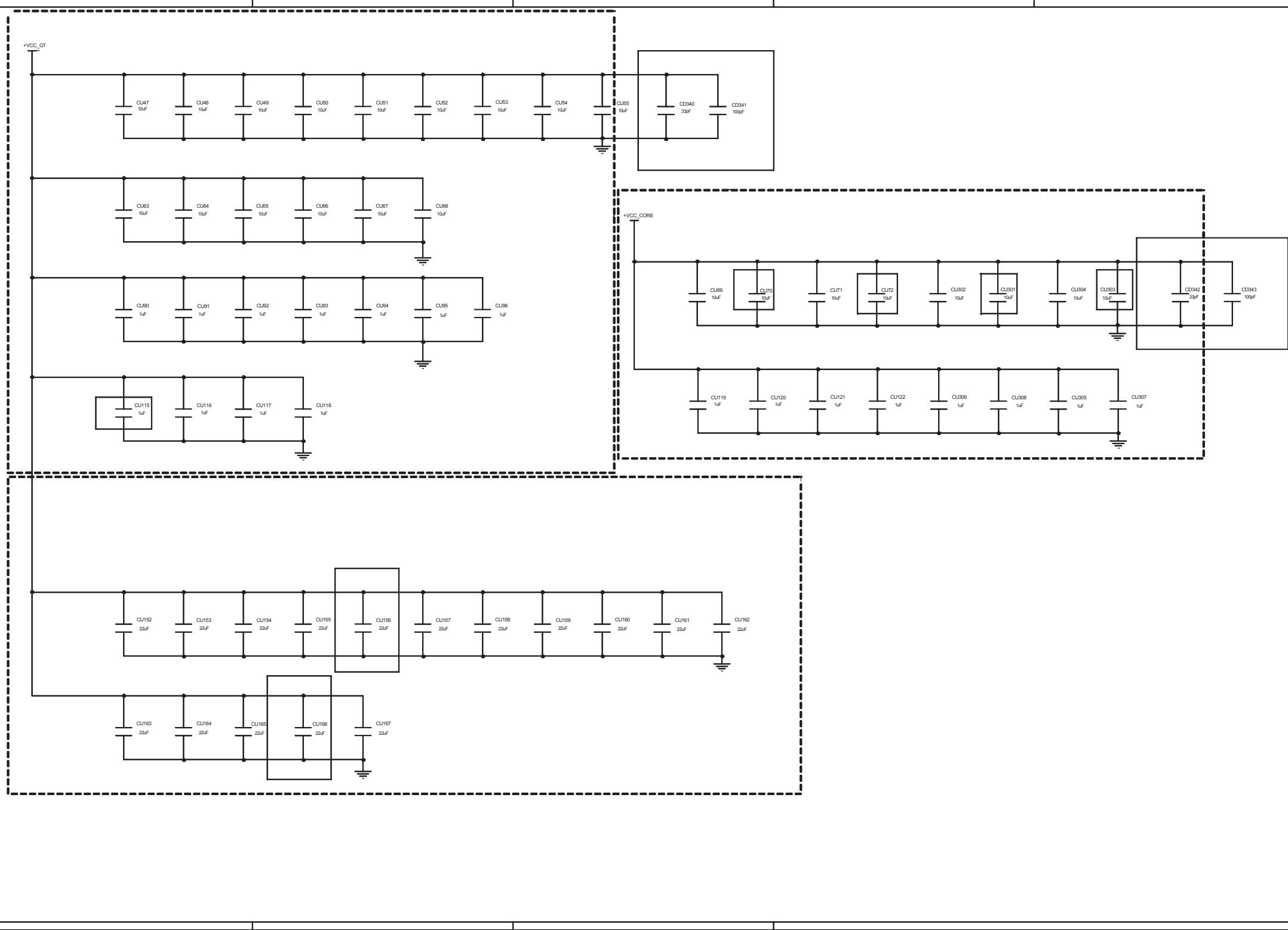


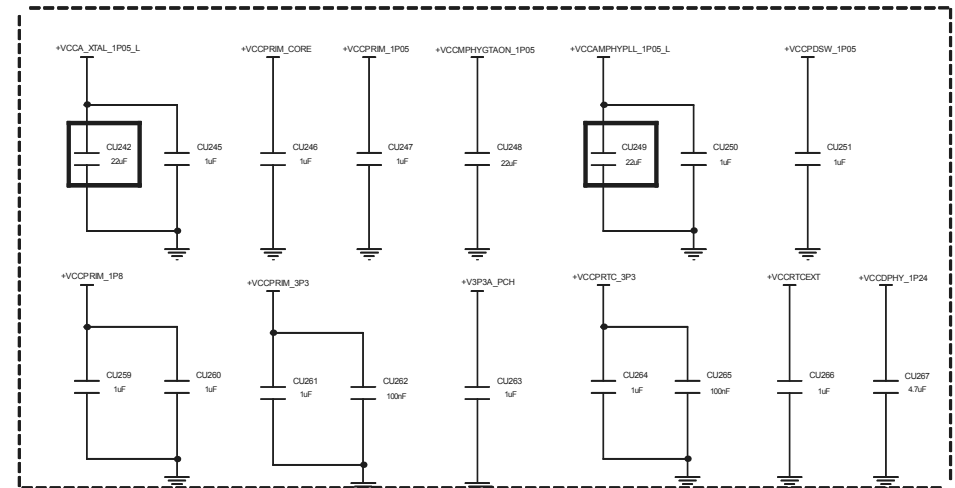
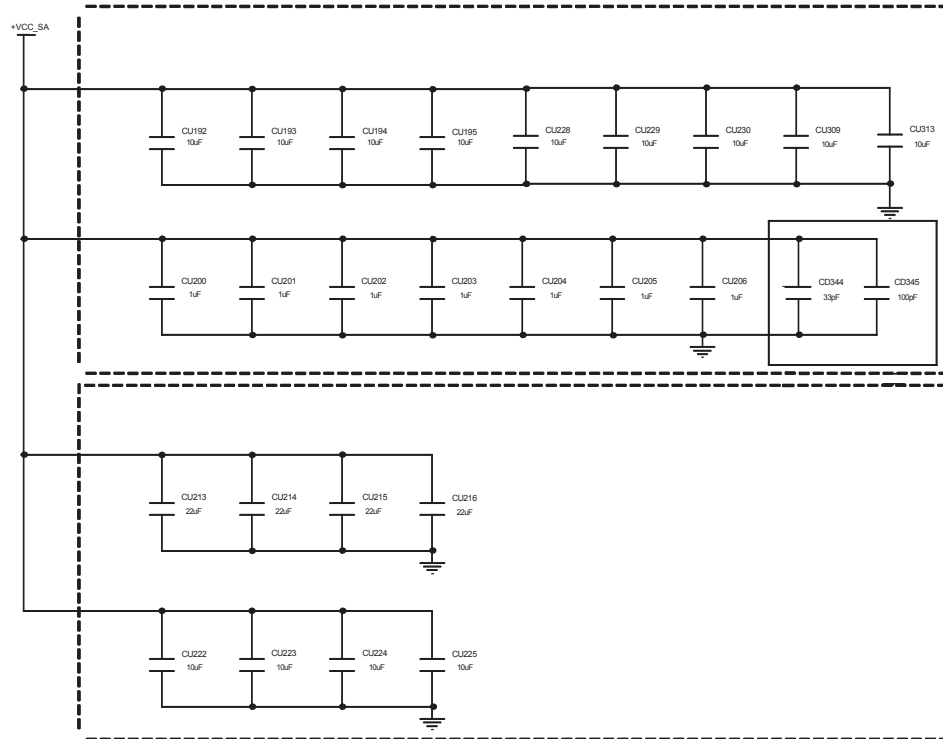


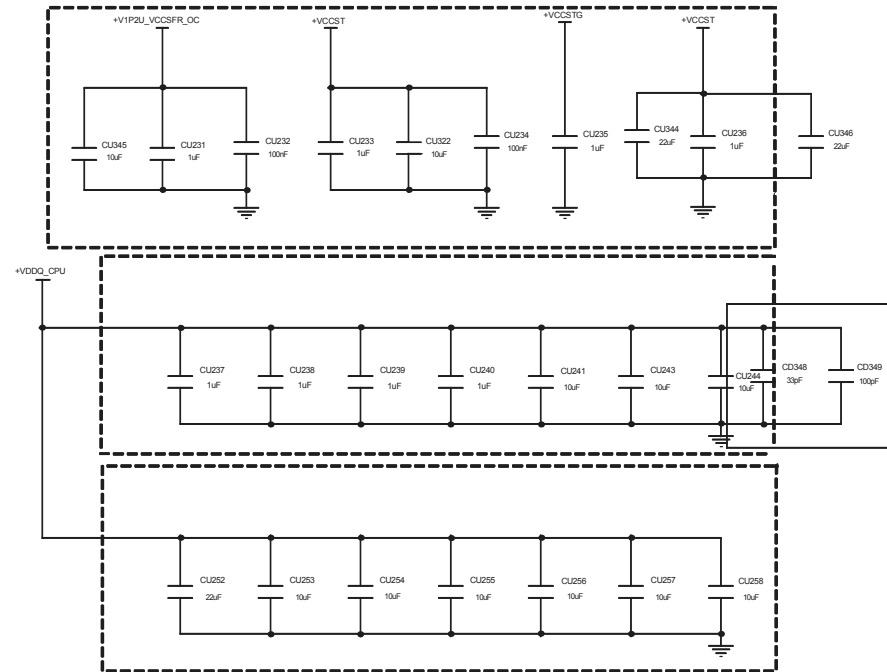
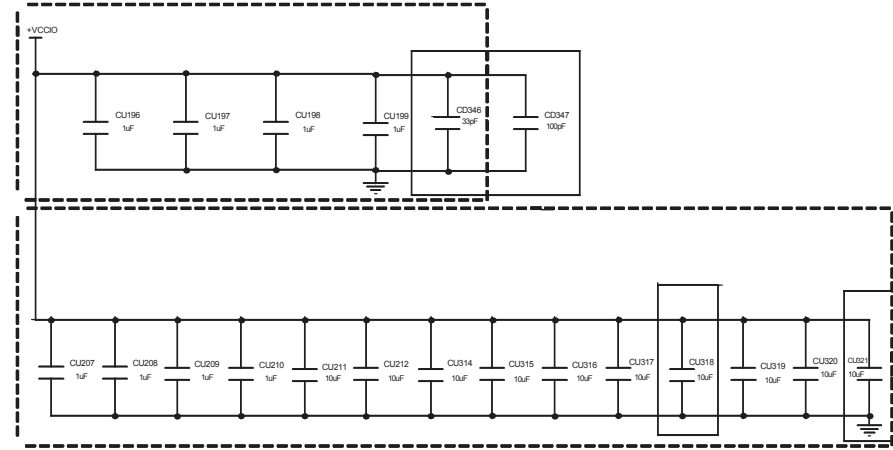


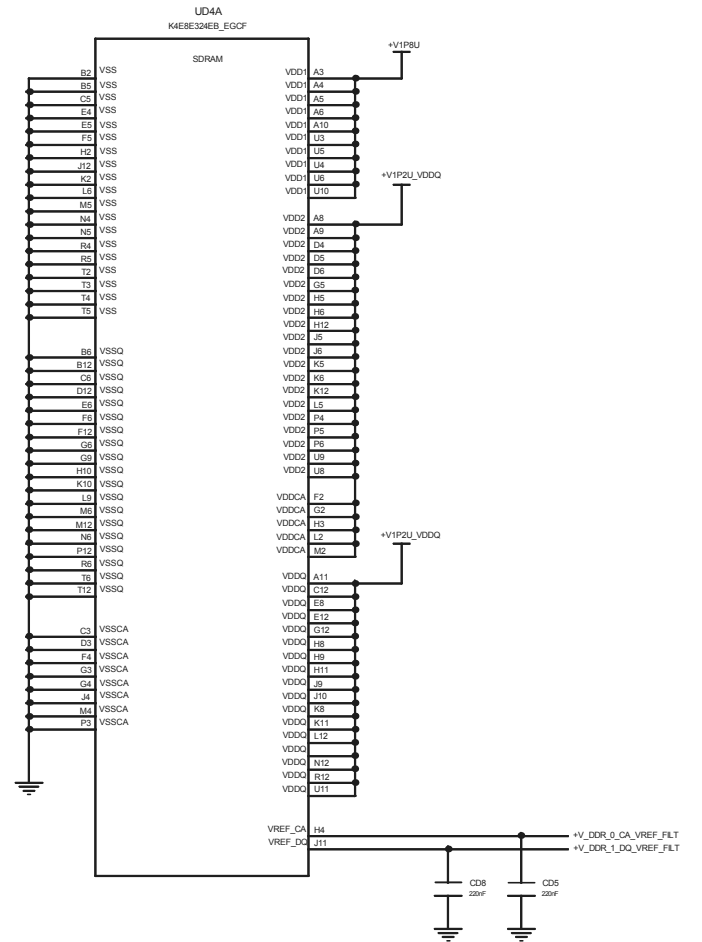
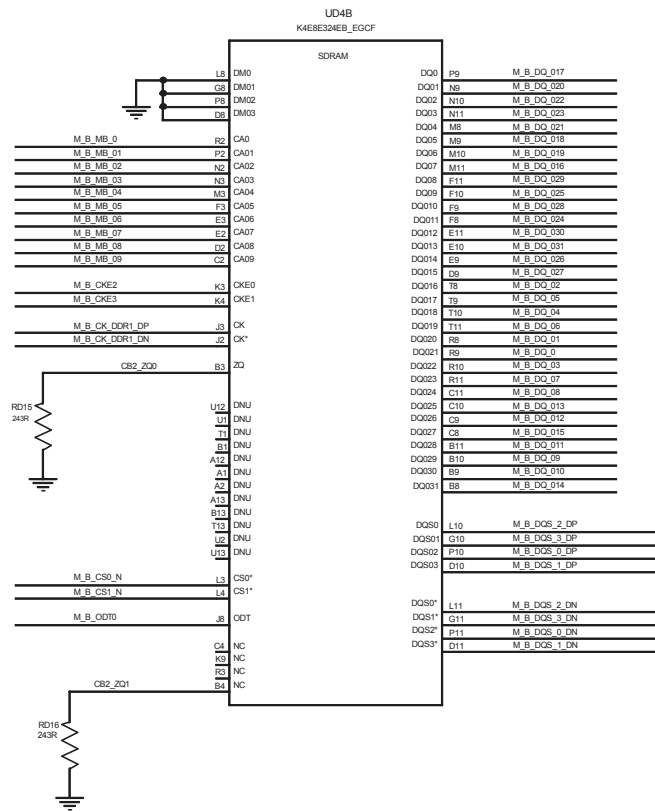
+VDD_CORE

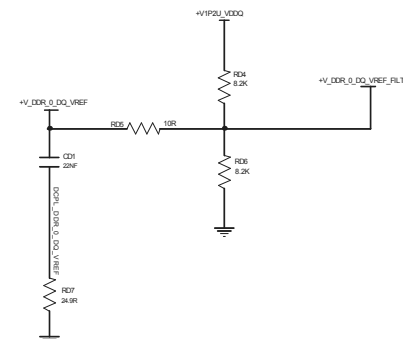
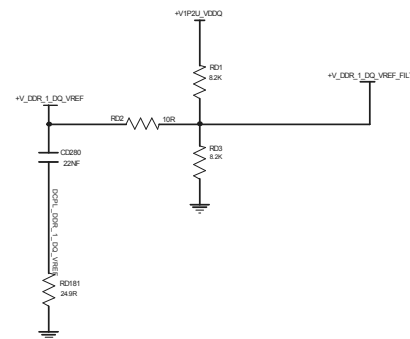
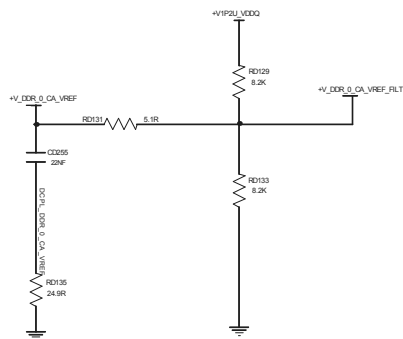
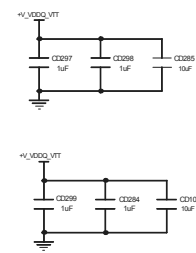
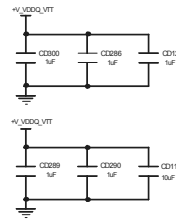
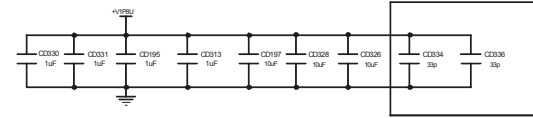
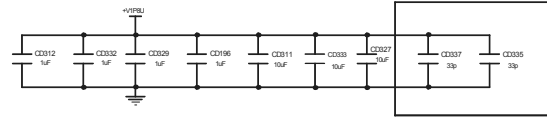
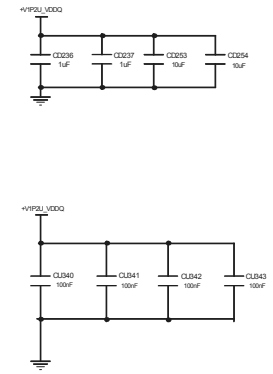
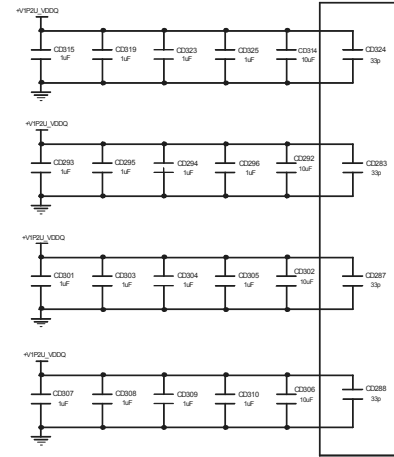
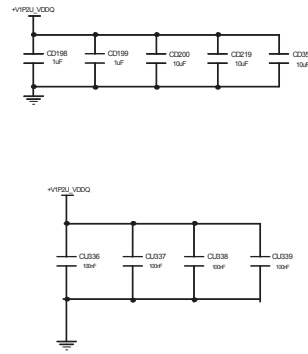
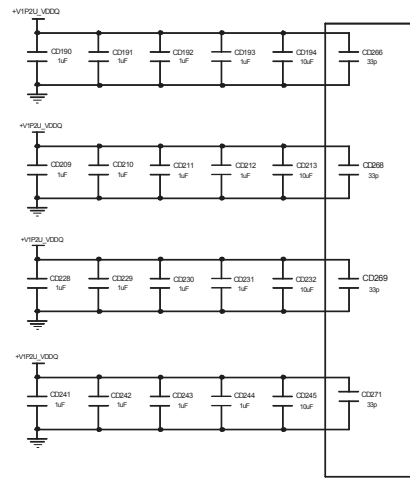


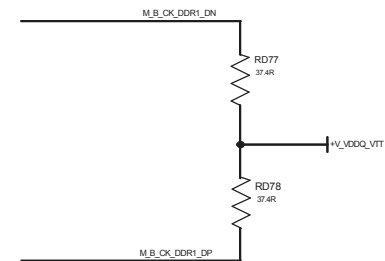
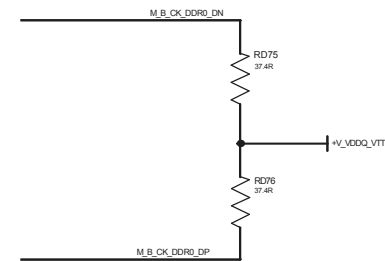
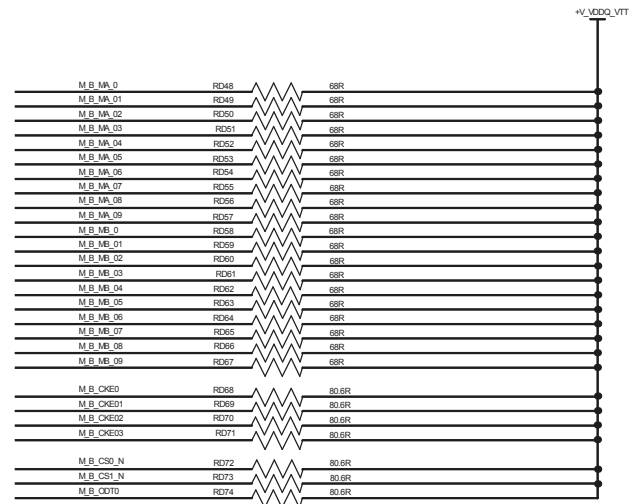
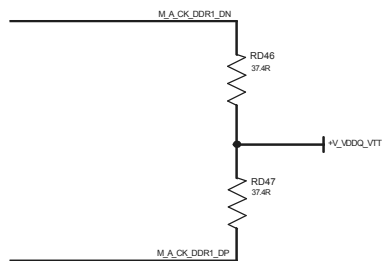
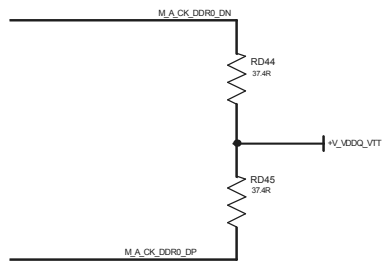
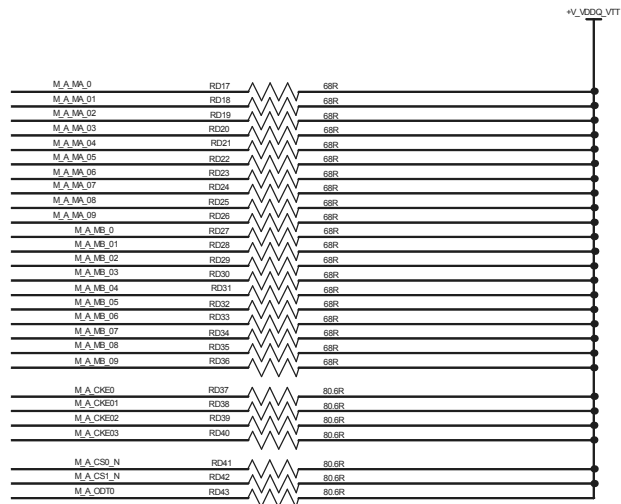


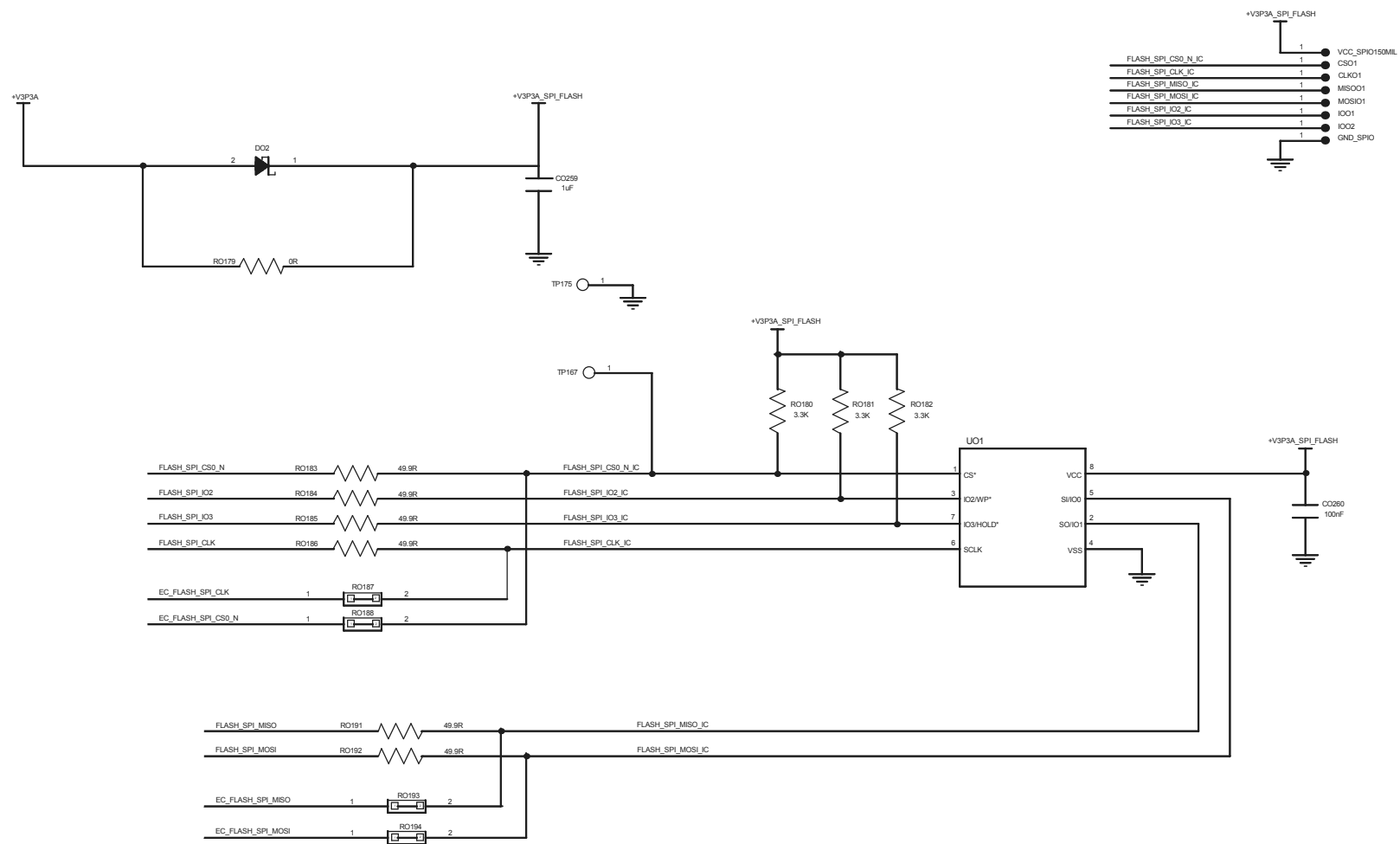


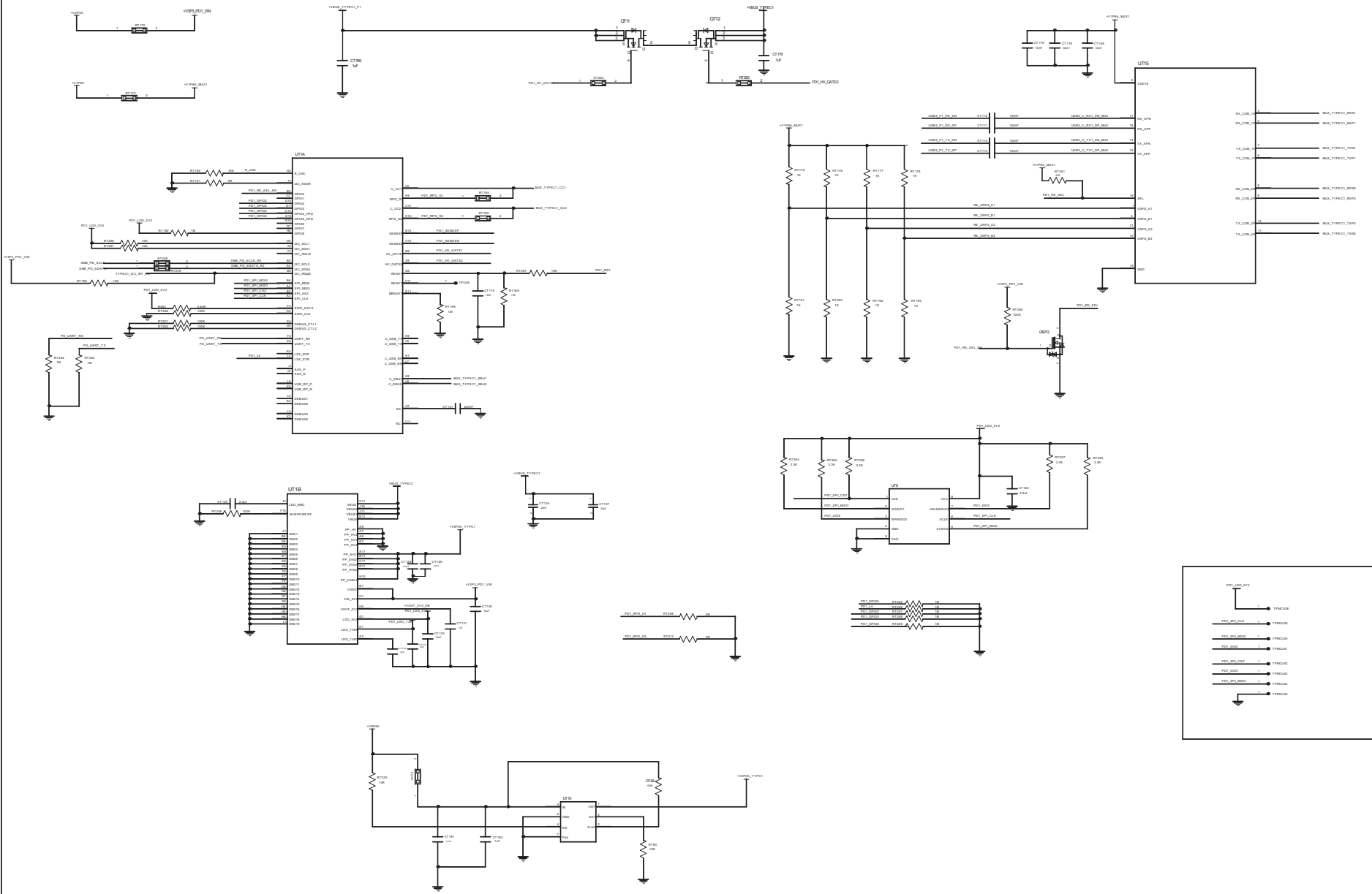


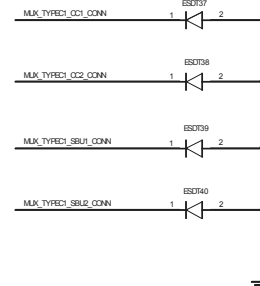
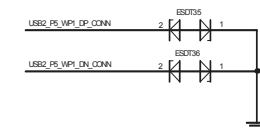
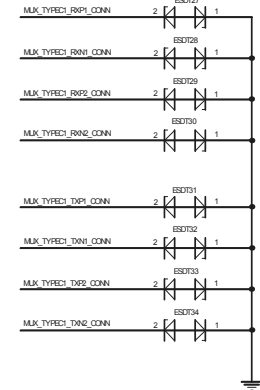
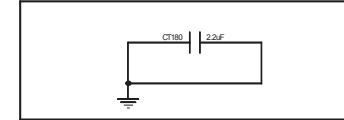
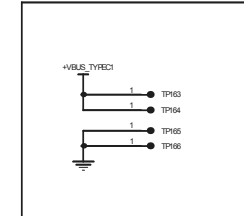
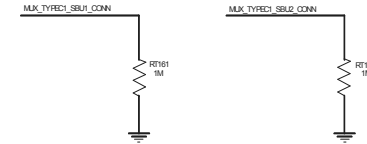
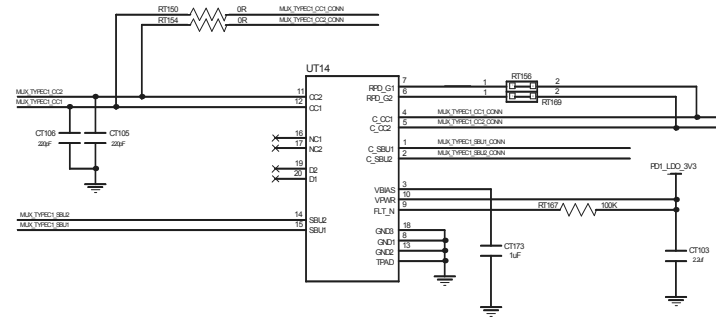
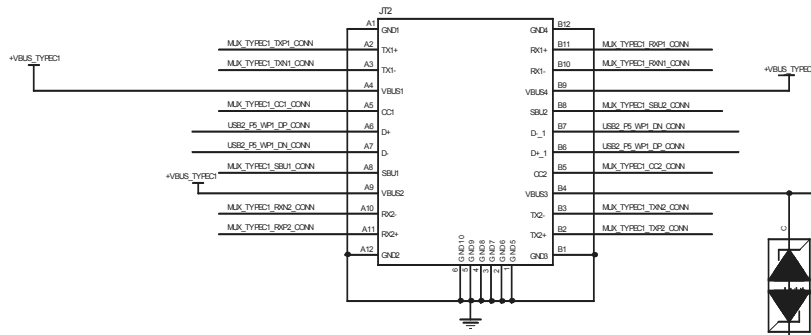
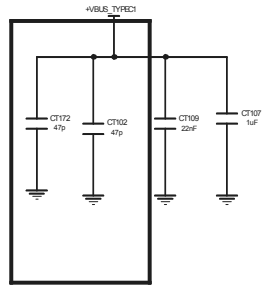
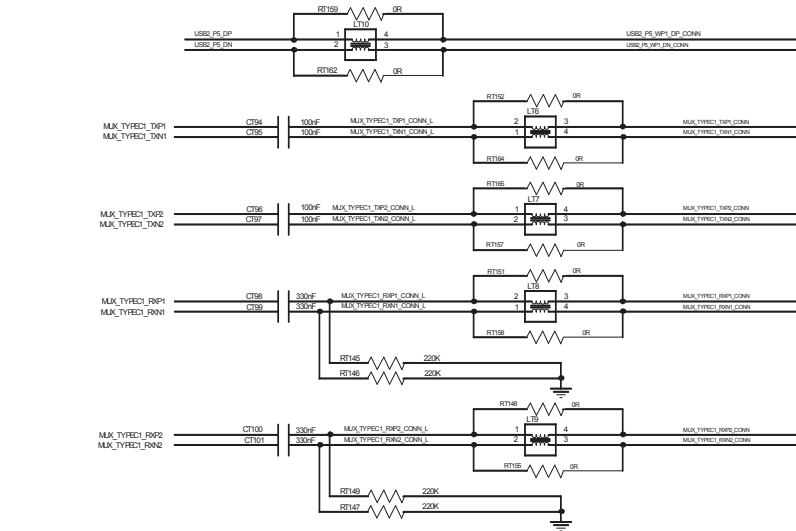


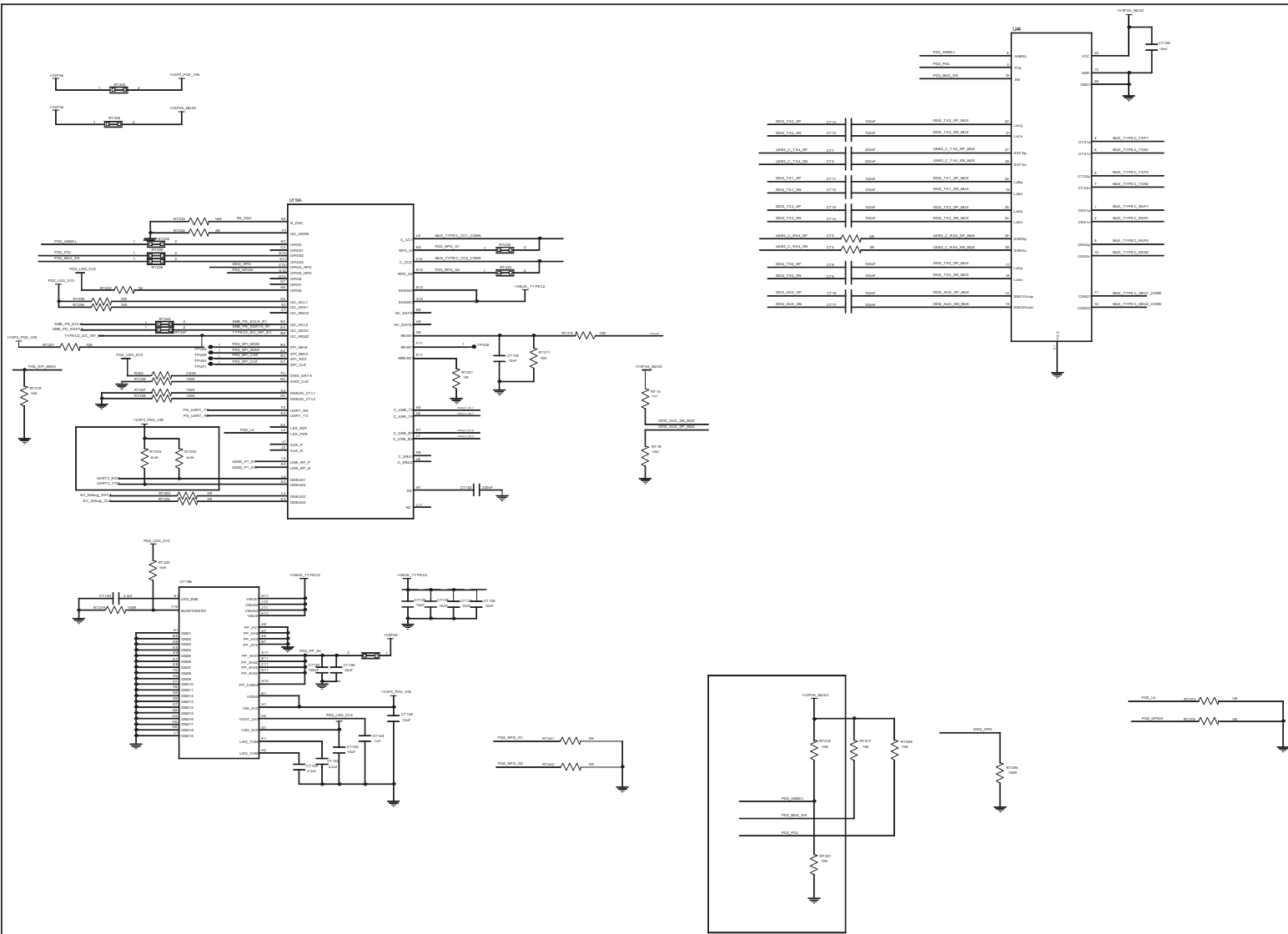


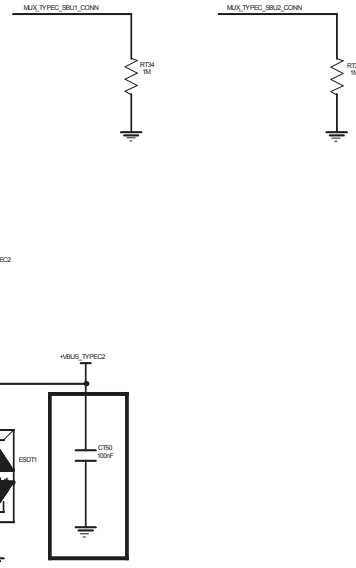
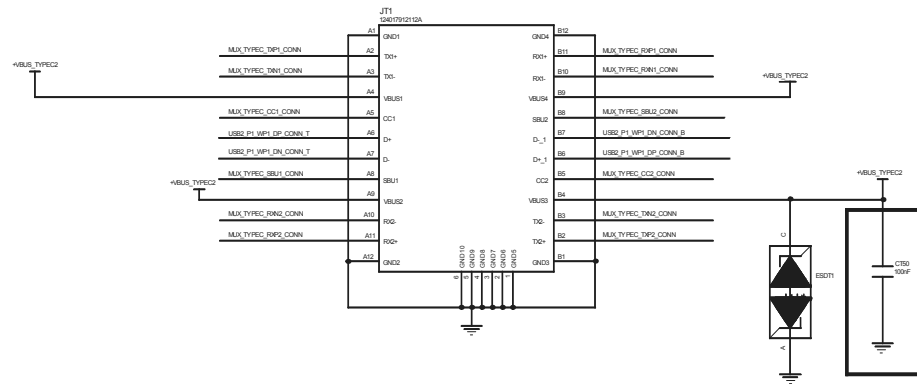
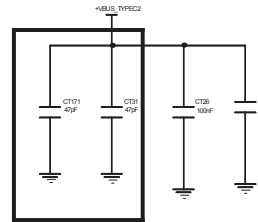
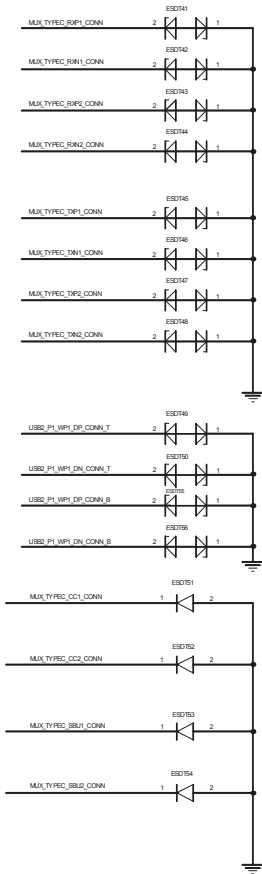
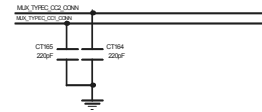
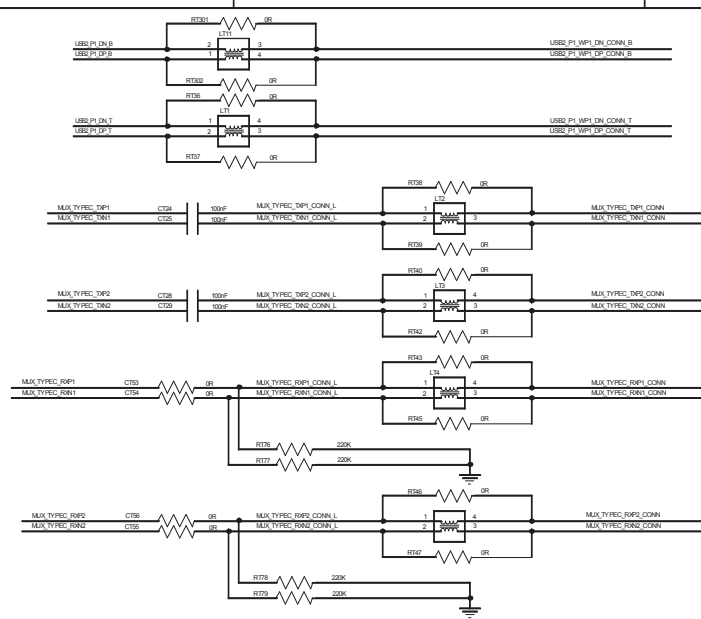




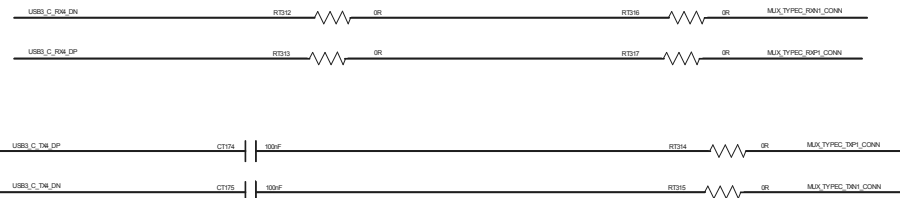






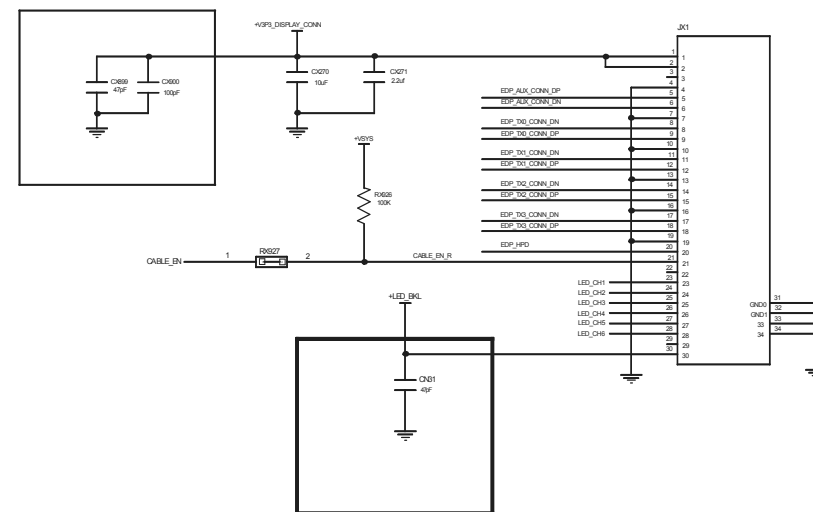
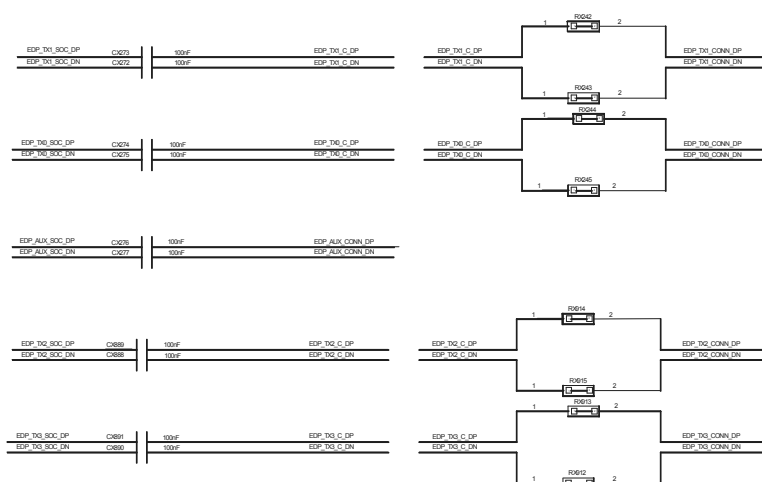


DCI Debug

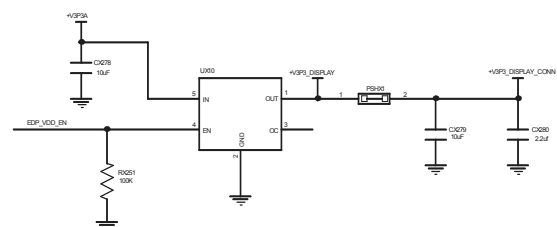


eDP Signal

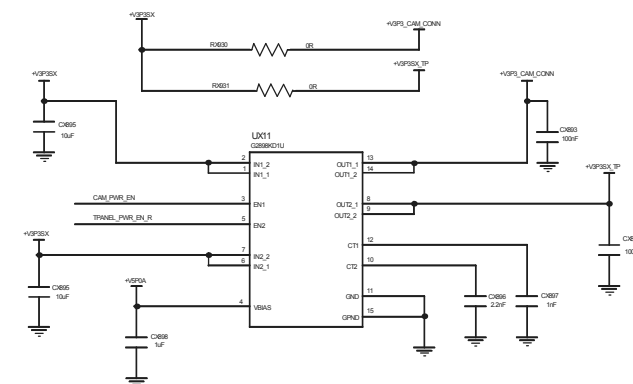
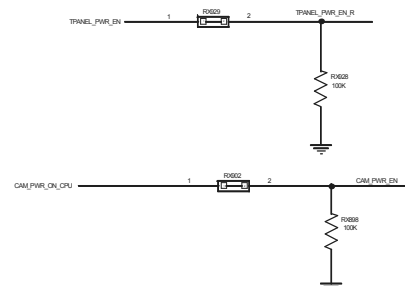
eDP & ALS CONN



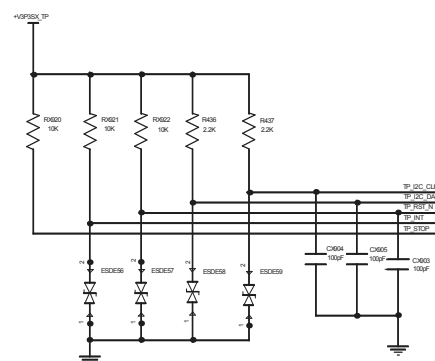
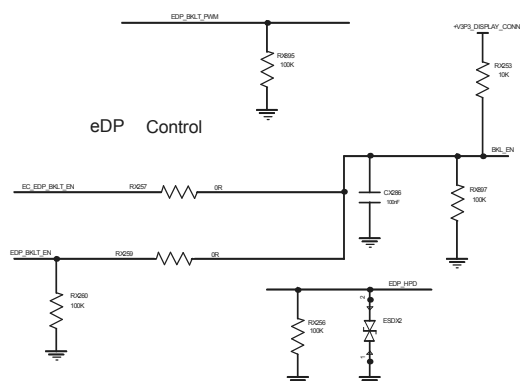
eDP	VCC	Power
-----	-----	-------



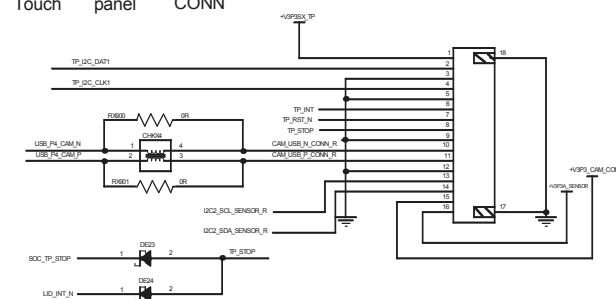
CAM Power

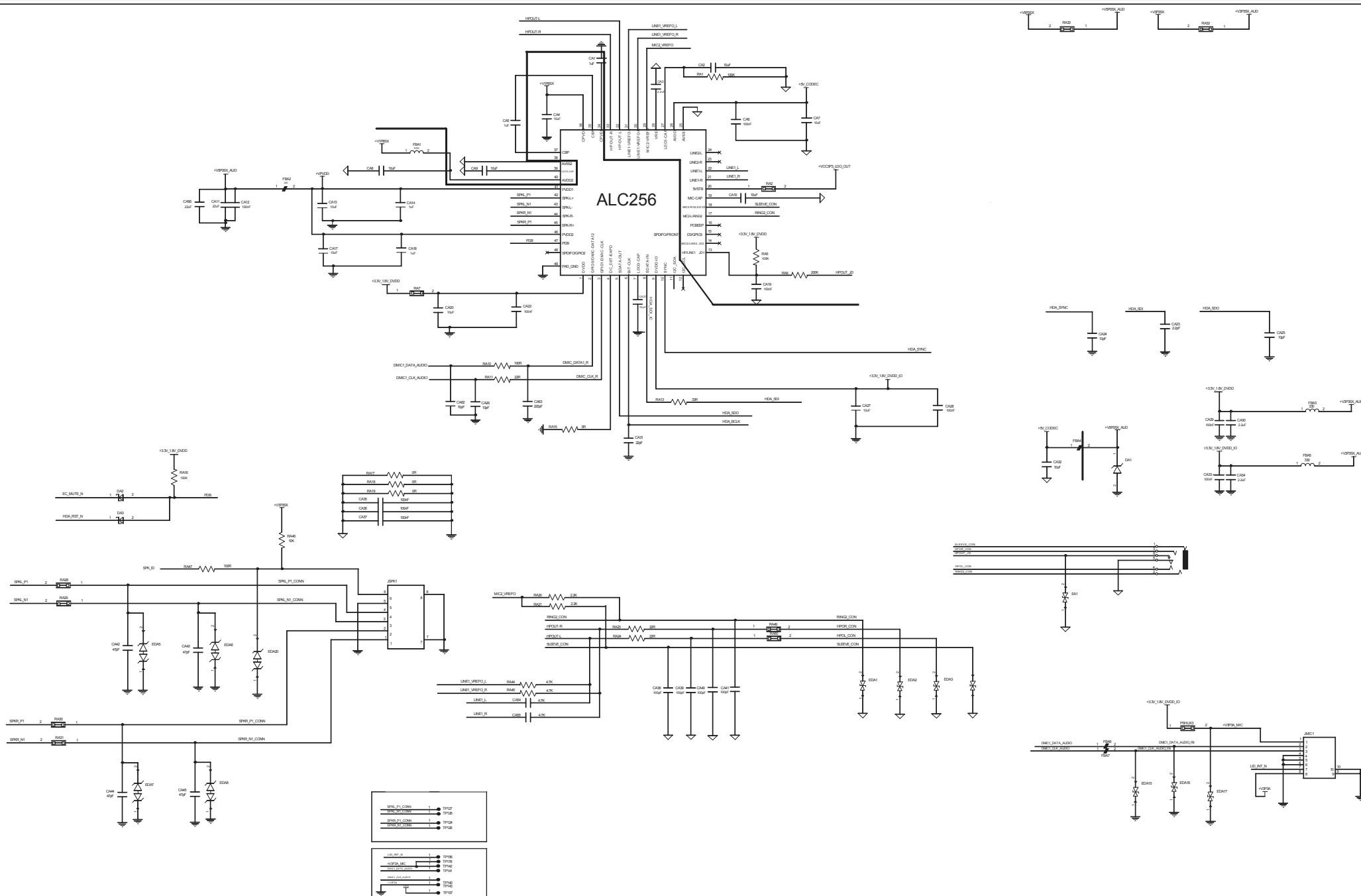


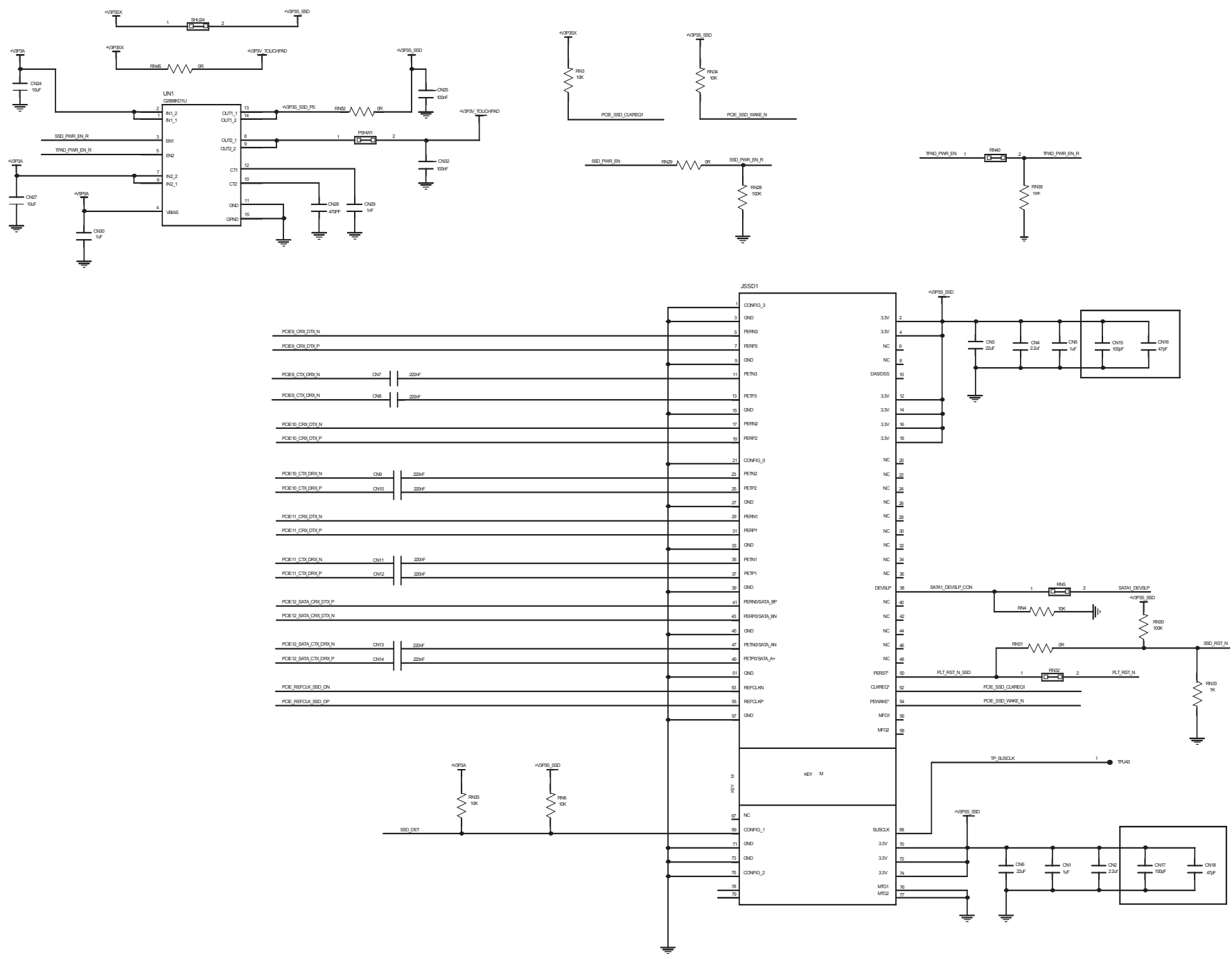
eDP	Control
-----	---------

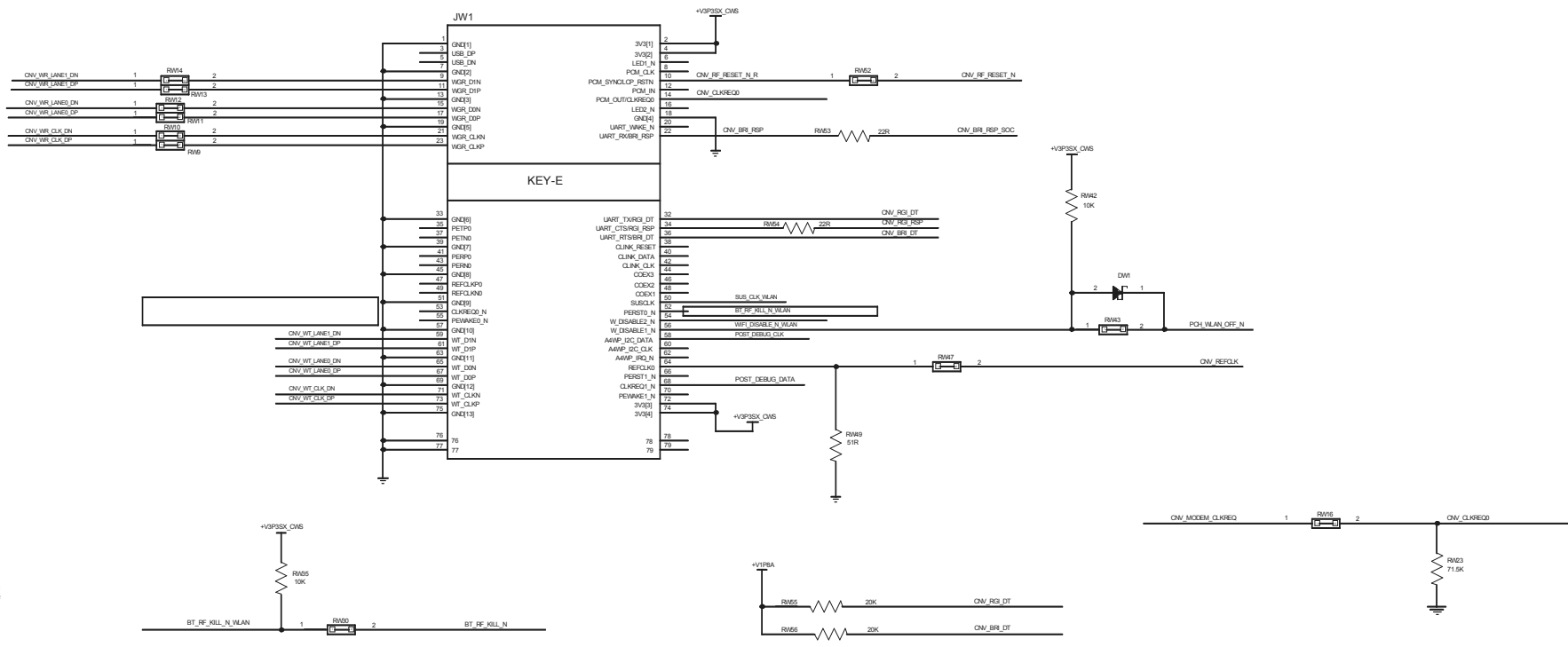


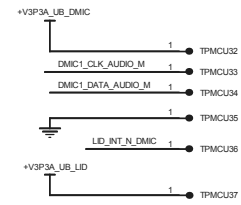
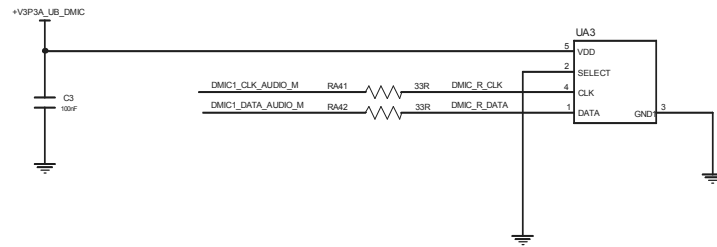
CAM & Touch panel CONN



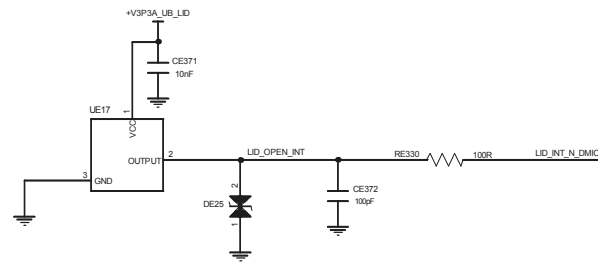




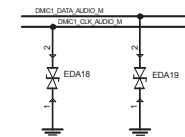
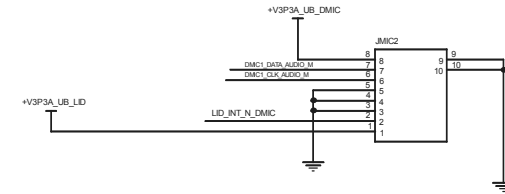
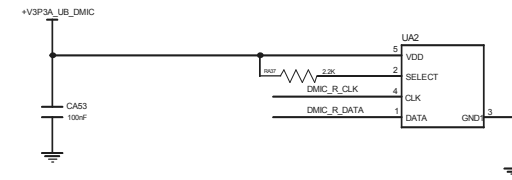




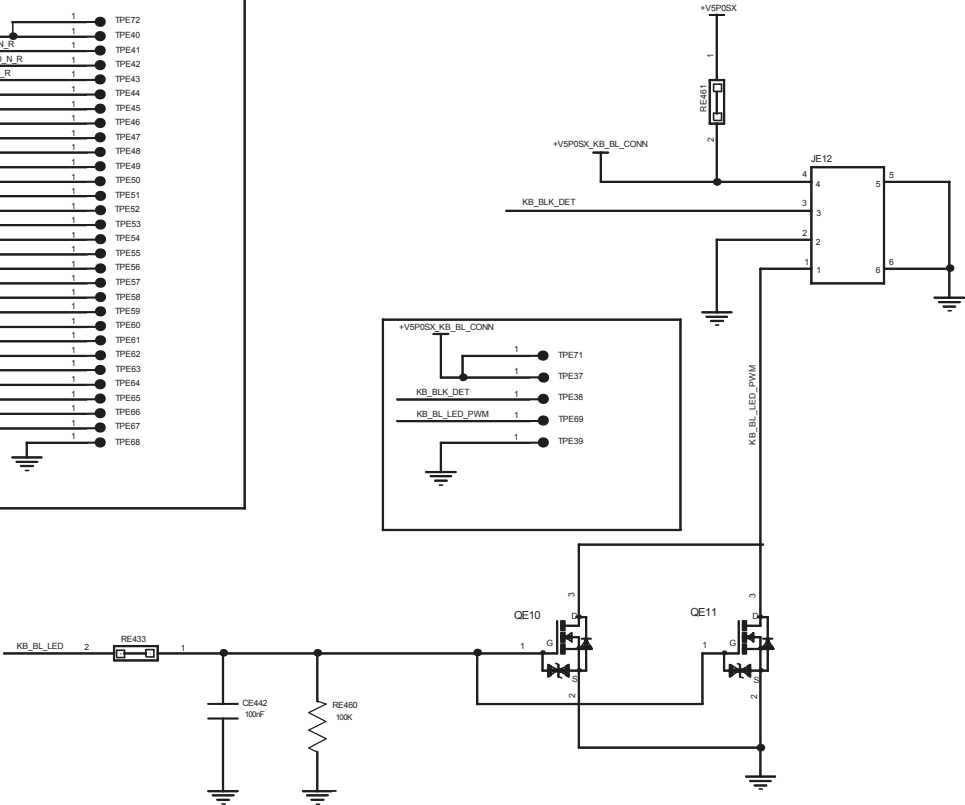
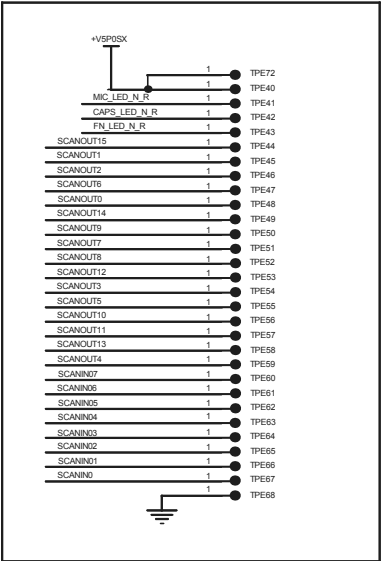
HALL



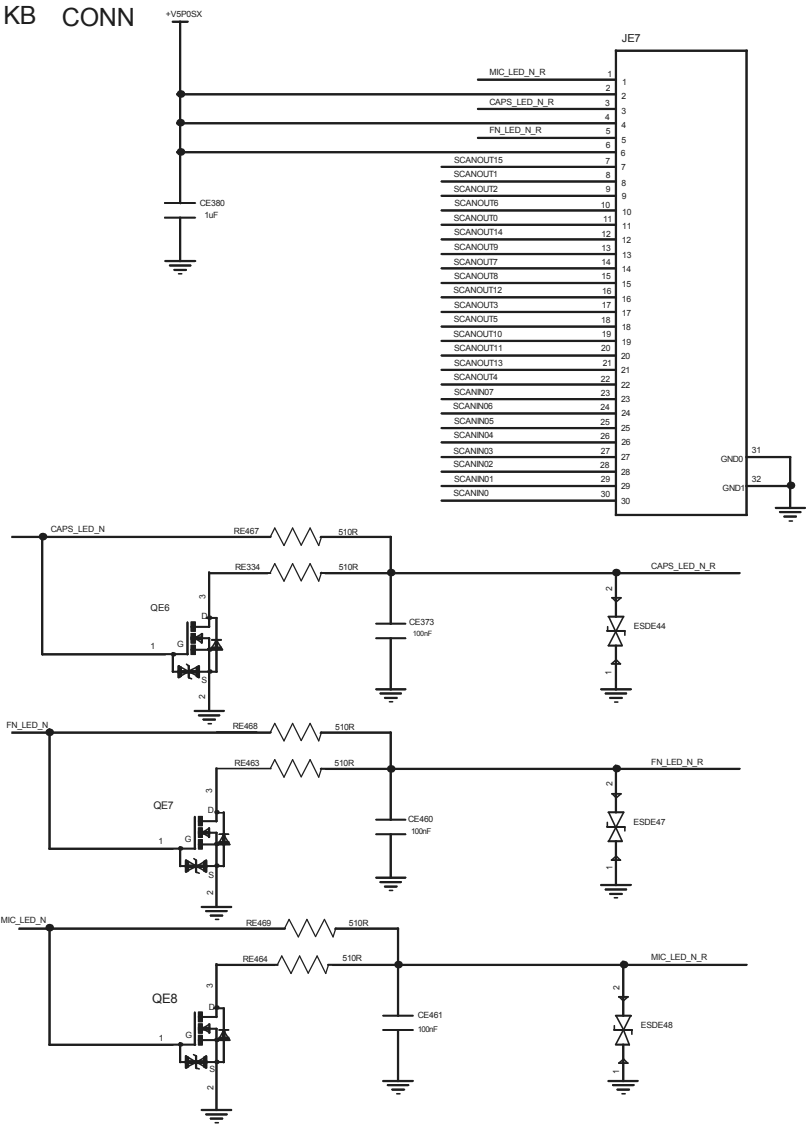
DMIC BOARD

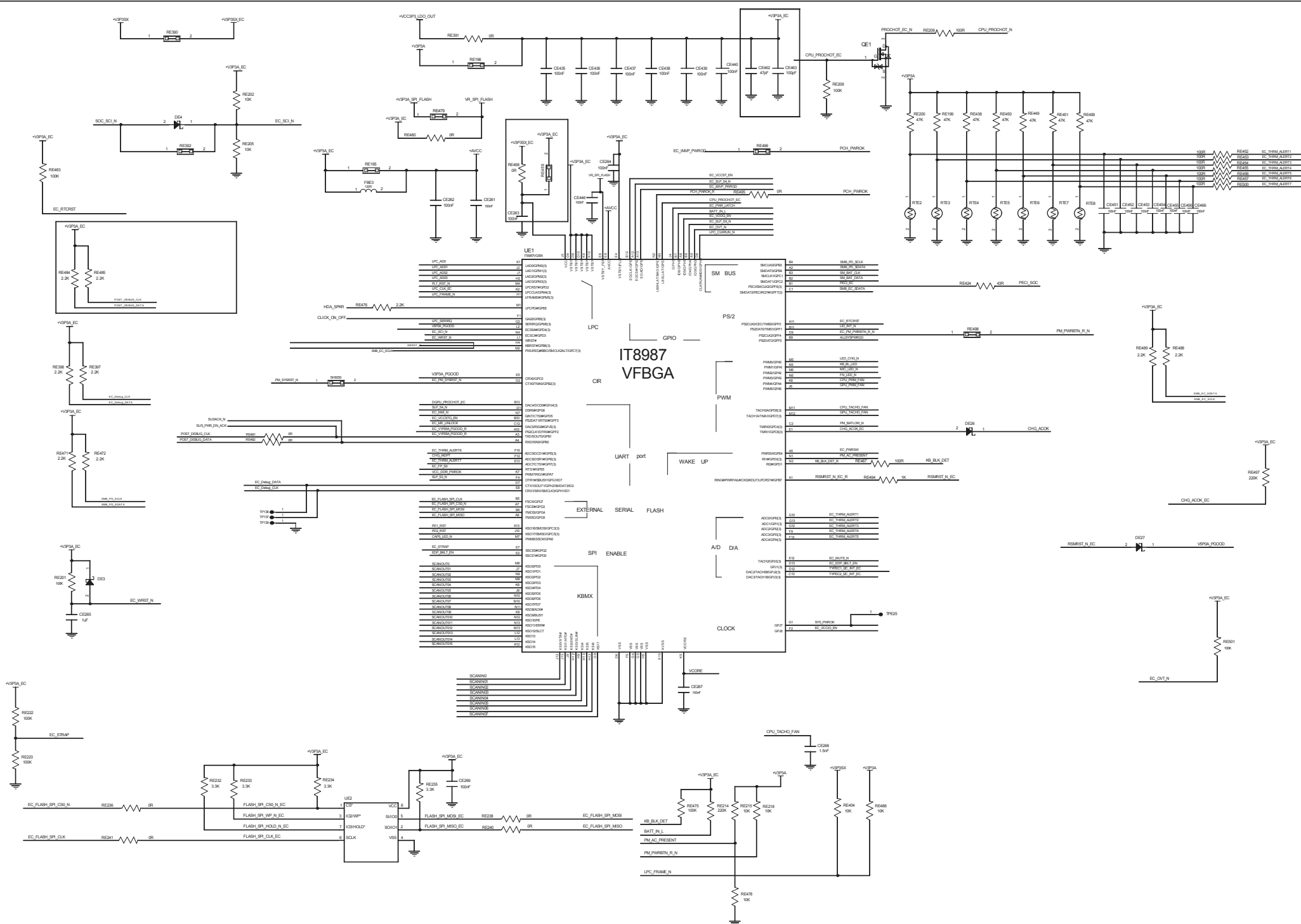


KB Backlight



KB CONN





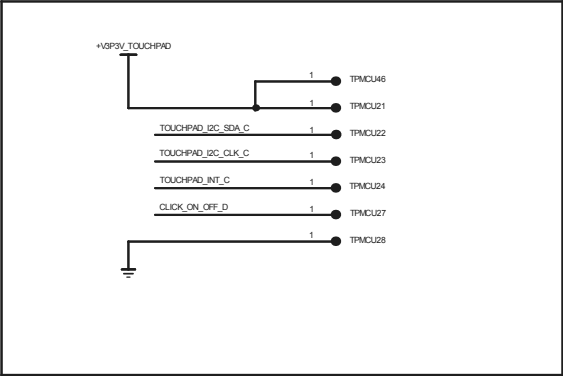
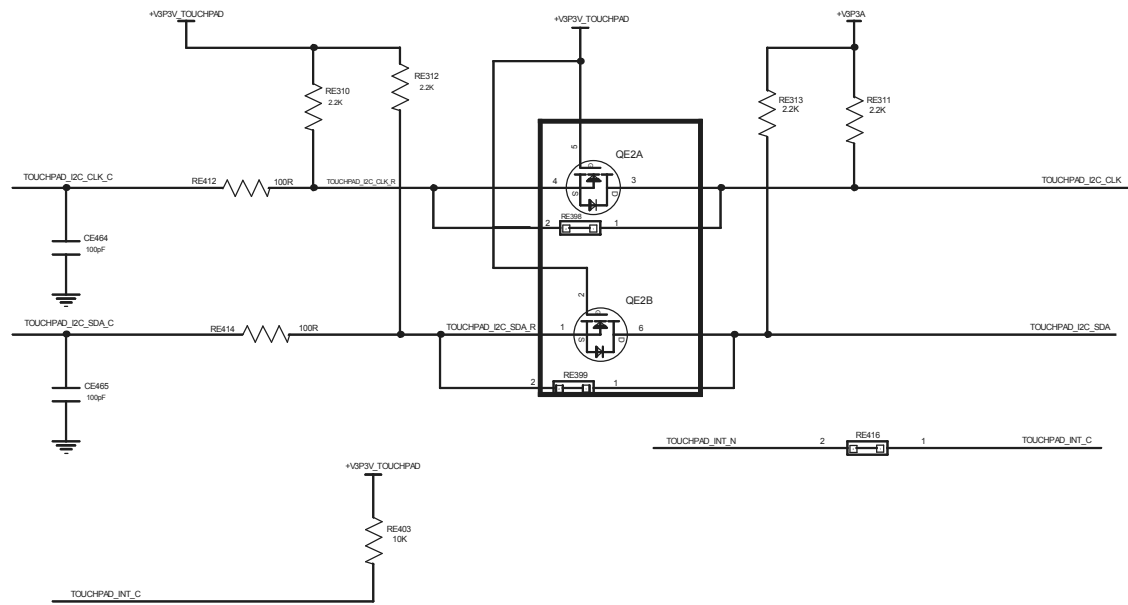
PWRBUTTON

The schematic diagram for the PWRBUTTON circuit shows a push-button labeled PBT_GNDIE1 connected to ground. The other terminal of the button is connected to a node labeled PWR_BUTTON_N. This node is also connected to three resistors: RE332 (10K) which is connected to +VCC3PS_LDO_OUT, RE335 (1K) which is connected to EC_PWRSW, and RE423 (1K) which is connected to PWRBTN_IN_N. A component labeled PBT_E1 is also connected to the PWR_BUTTON_N node.

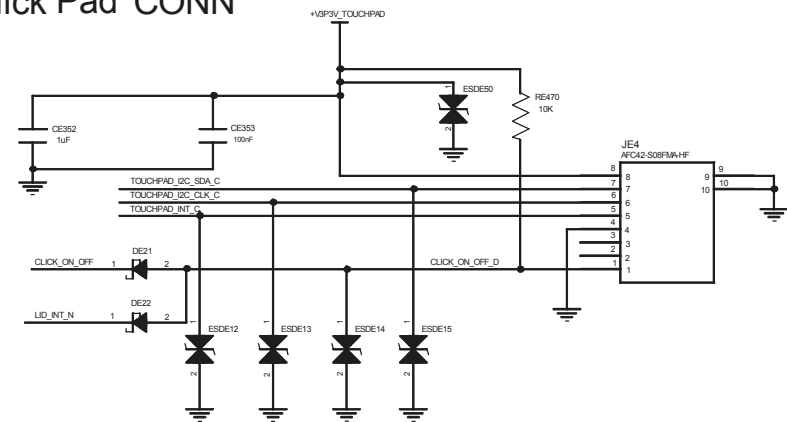
The schematic diagram illustrates the WRBUTTONLOGIC circuit. It features several input signals and components:

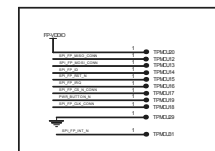
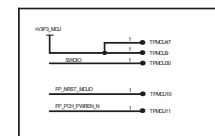
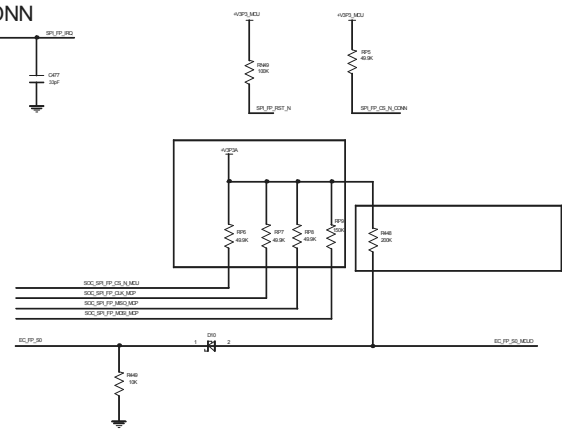
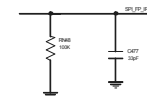
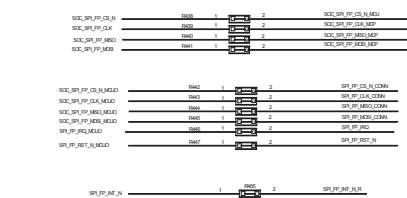
- +VCC3P3_LDO_OUT**: A power supply input connected to resistor R56 (10K) and resistor R58 (1K).
- +V3P3A**: A power supply input connected to resistor R71 (10K).
- EC_PWRSW**: An input signal connected through resistor R70 to pin 1 of diode D3.
- PWRBTN_IN_N**: An input signal labeled "OPEN/DRN" connected through resistor R467 (2M) to pin 2 of diode D5.
- +VBUS_TYPEC1_P1**: An input signal connected through resistor R63 (2M) to pin 2 of diode D6.
- VNDP_EC_PWR_R**: An input signal connected to pin 2 of diode D6.
- EC_PMR_LATCH**: An input signal connected to pin 2 of diode D7.
- TP176** and **TP162**: Test points connected to ground.
- R57** (10K) and **C22** (1uF): A network connected to the +V3P3A supply and the V3P3A_DISABLE pin of MOSFET Q2.
- D4**, **D5**, **D6**, and **D7**: Diodes used for signal conditioning and protection.
- Q2**: A MOSFET (Q6211) whose gate is driven by the logic circuit and whose drain is connected to +VCC3P3_LDO_OUT. Its source is connected to the 3P3VA_EN pin.
- R55** (1M) and **C100** (1uF): A network connected to the EC_PMR_LATCH_D pin and ground.
- R59** (10K) and **C25** (220nF): A network connected to the 3P3VA_EN pin and ground.

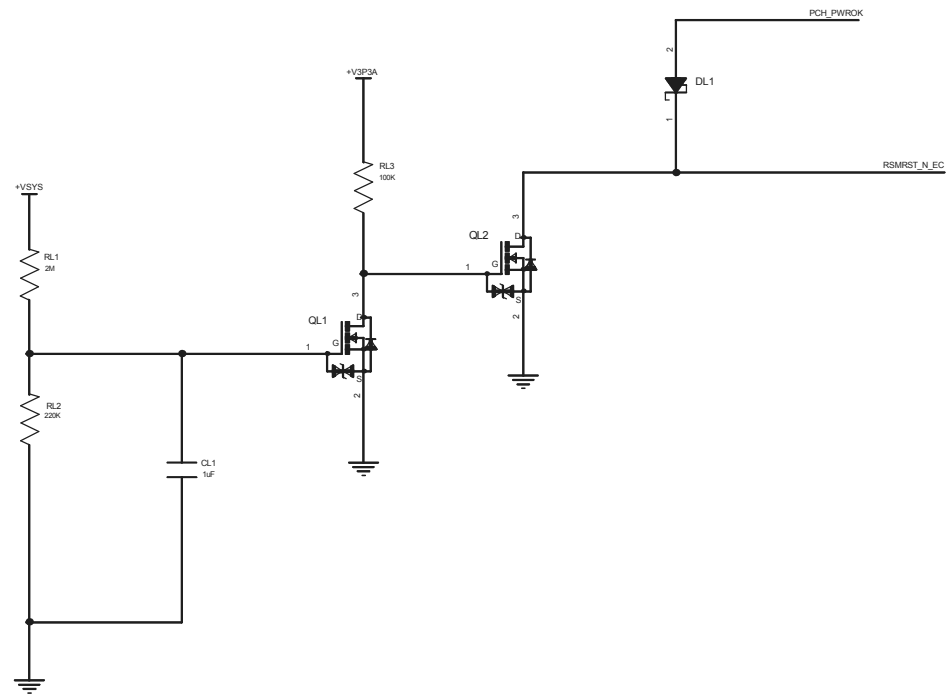
Touch Pad

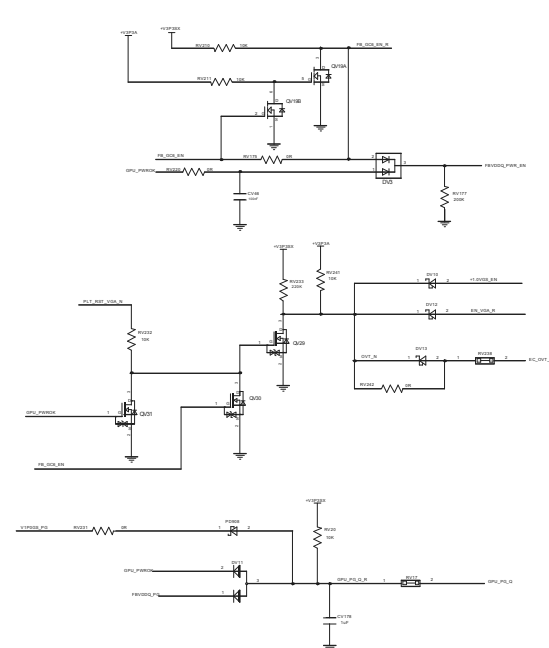
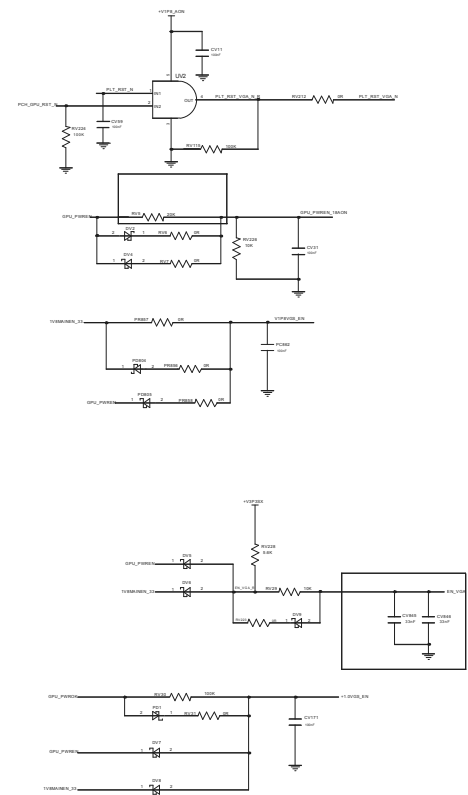
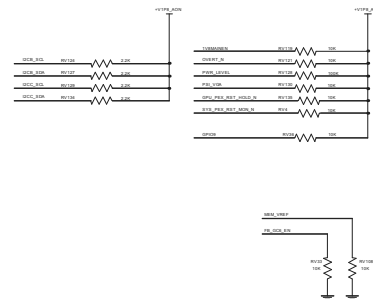
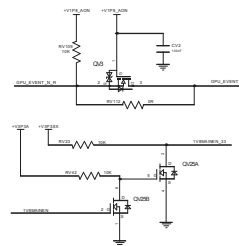
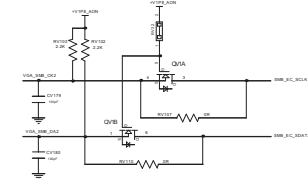


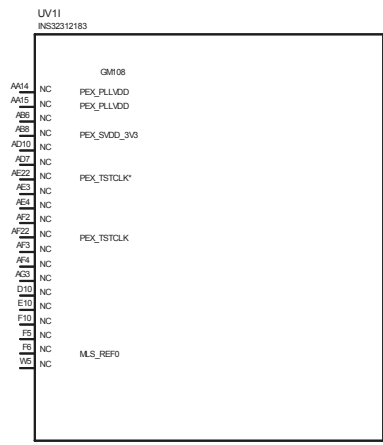
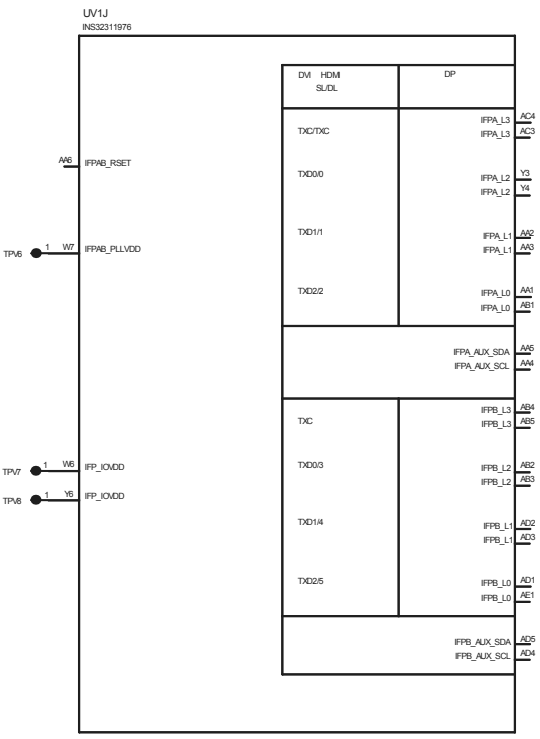
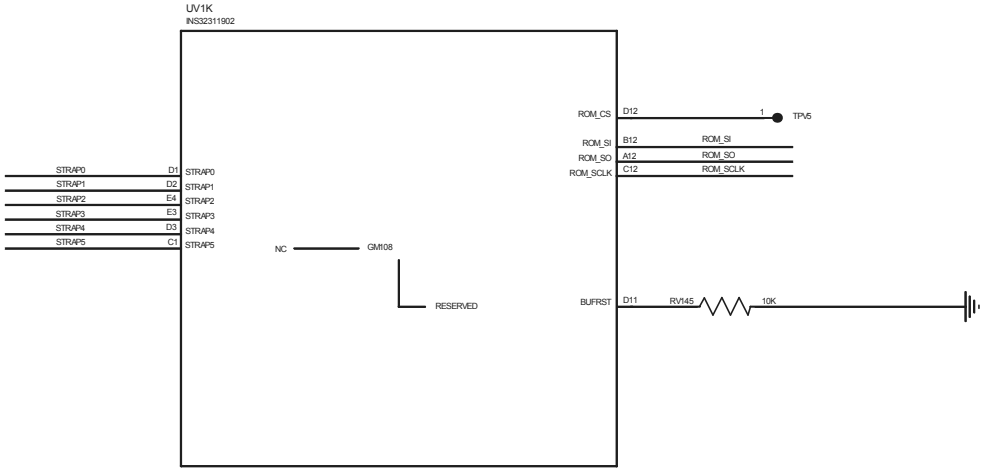
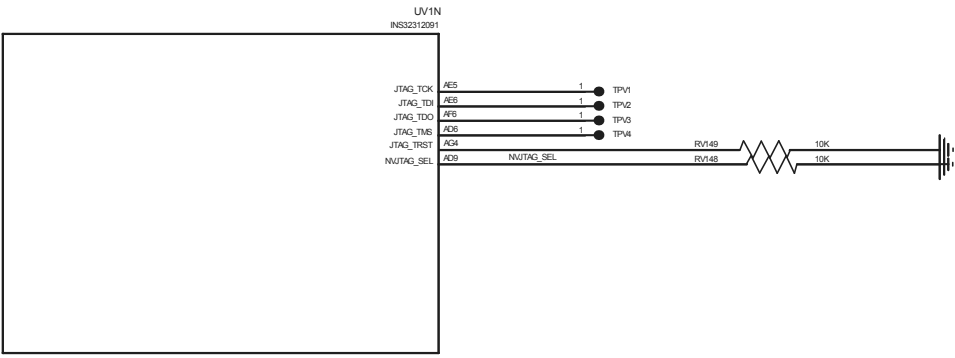
Click Pad CONN

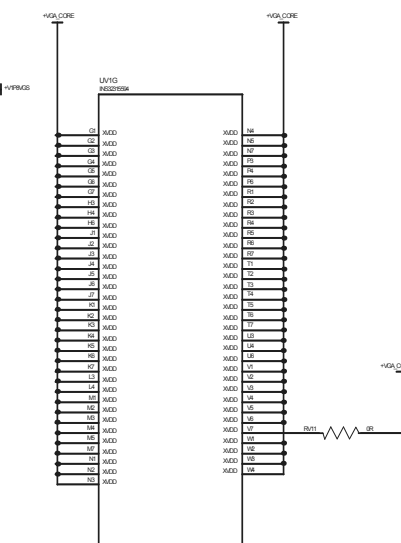
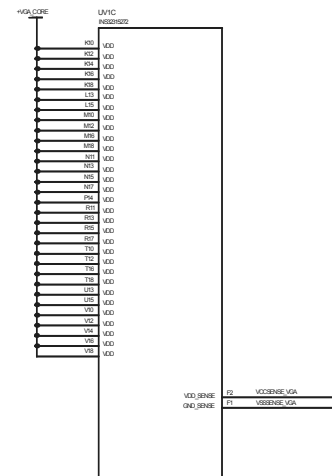
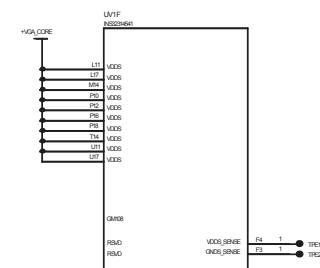
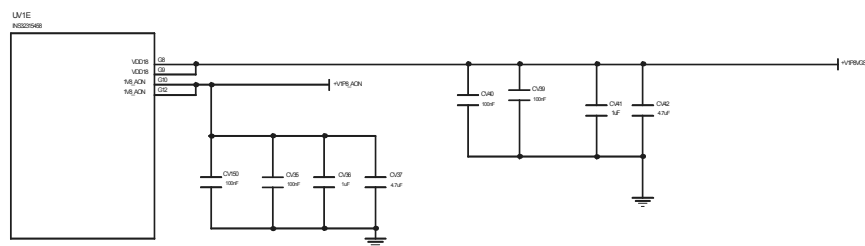


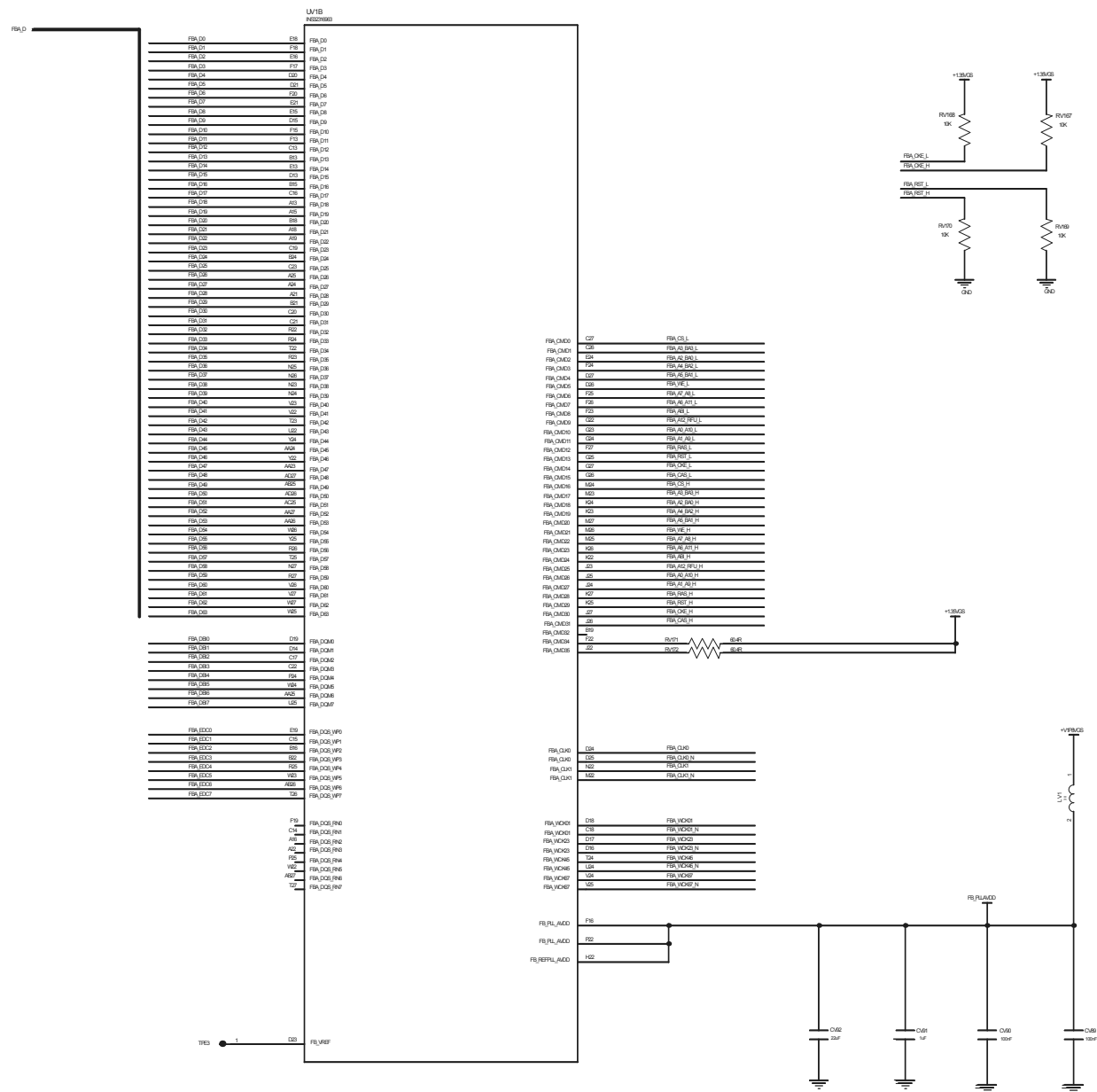


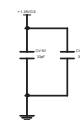
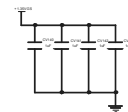
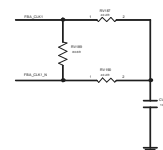
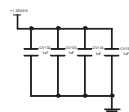
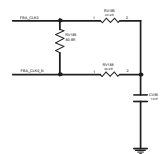
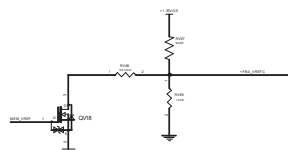


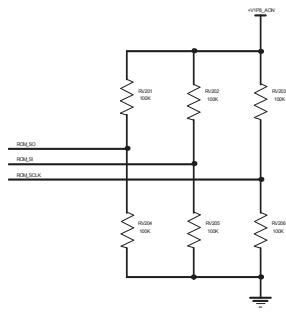
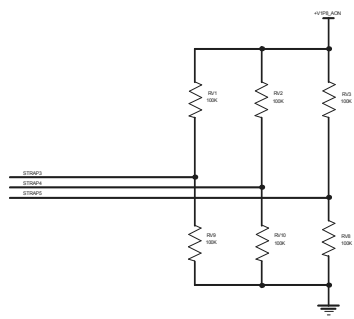
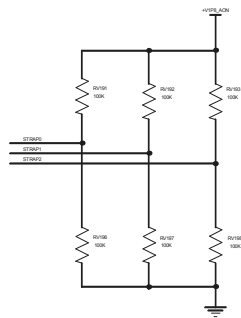


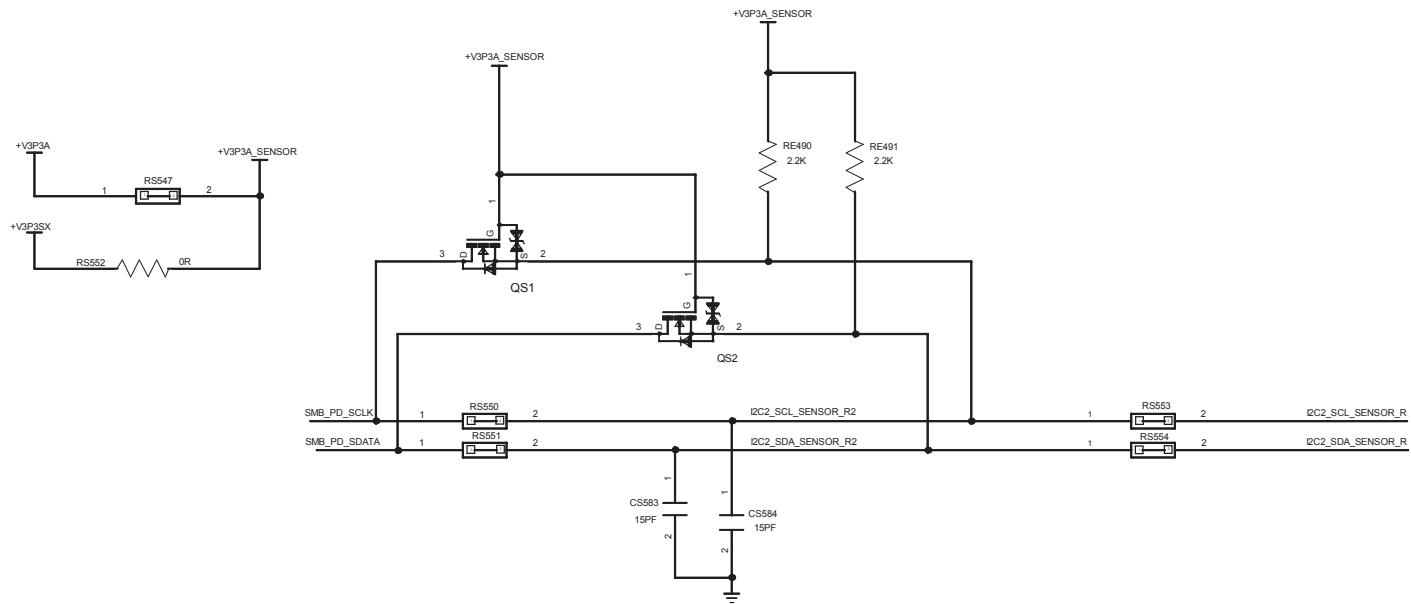


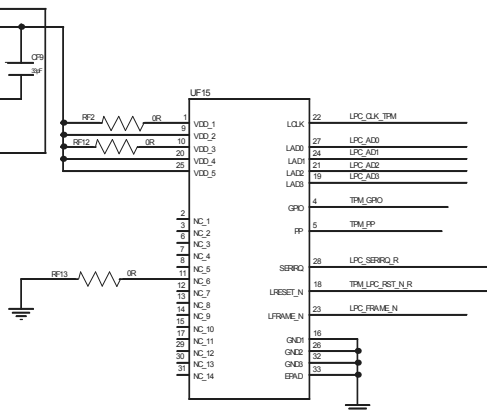
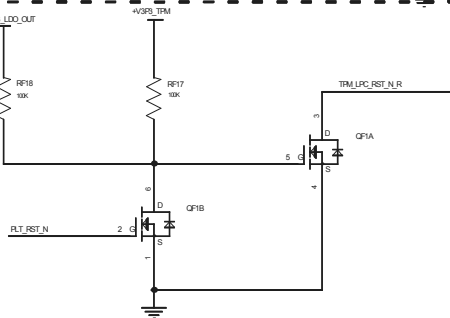
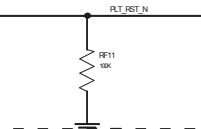
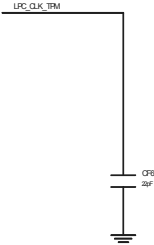


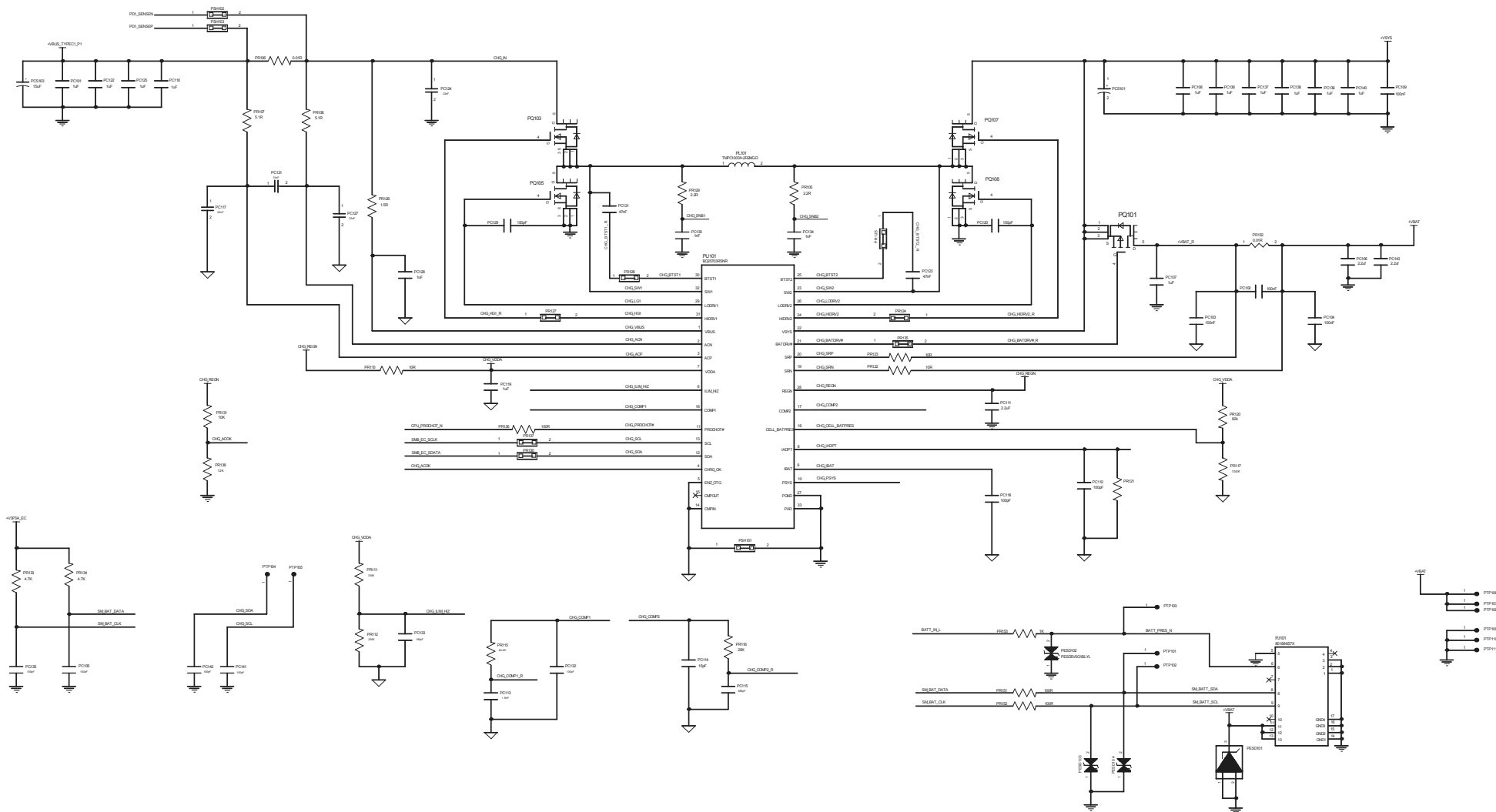


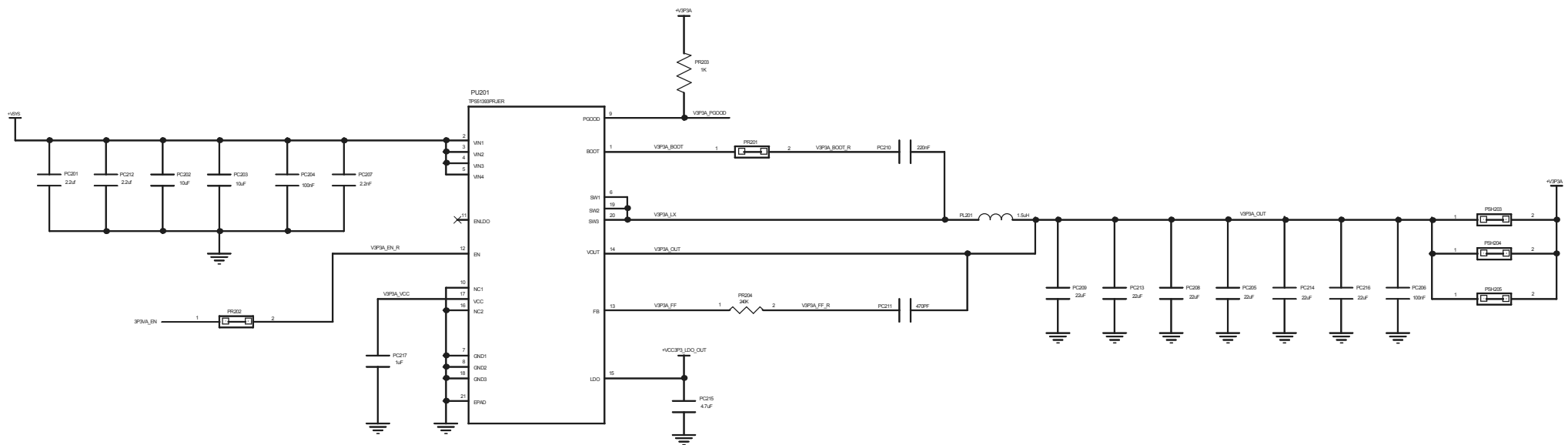


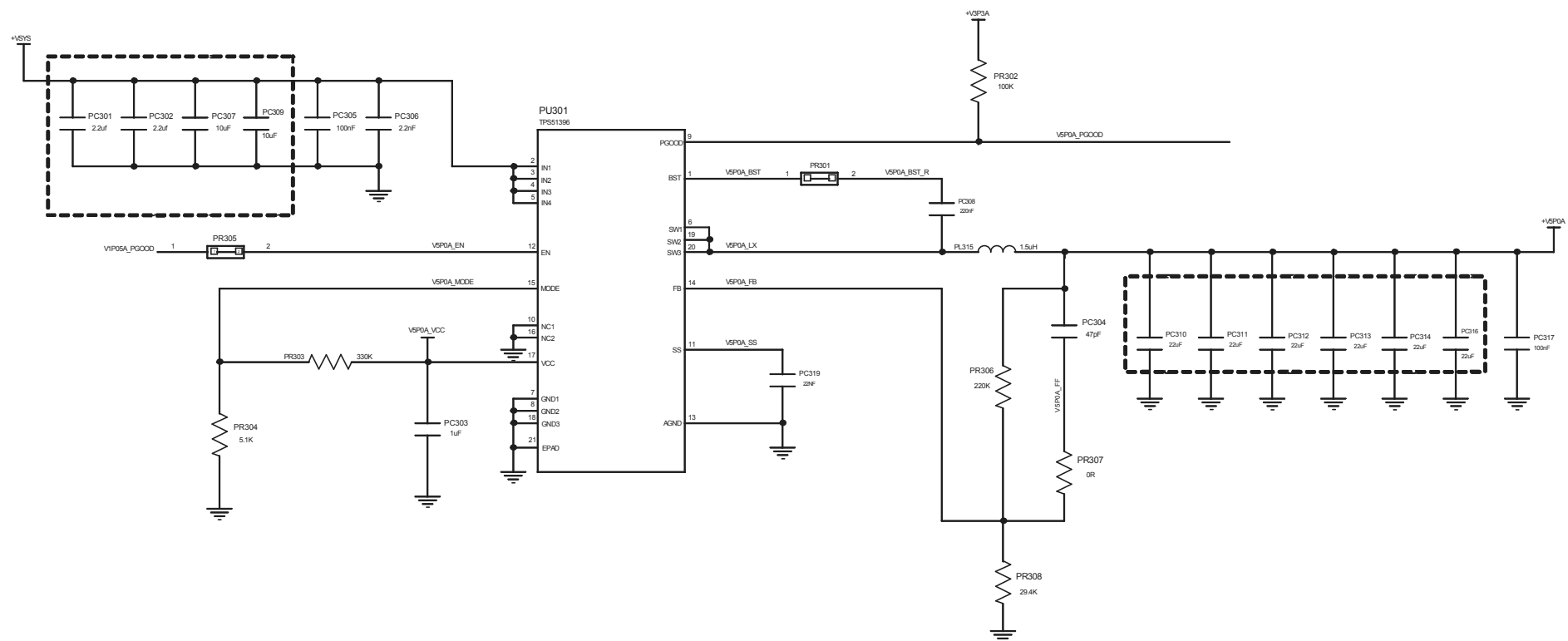


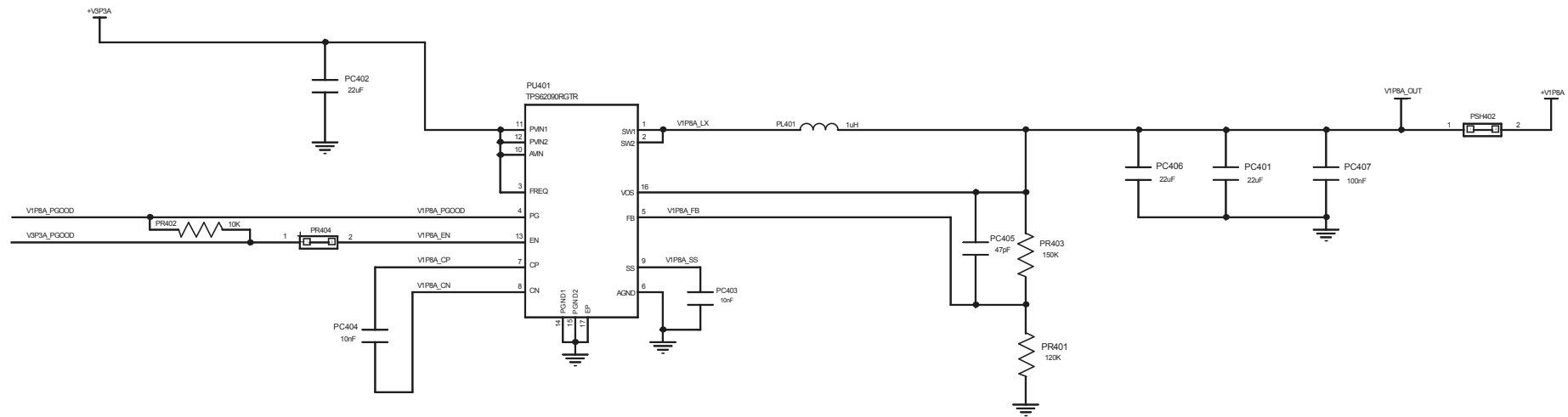


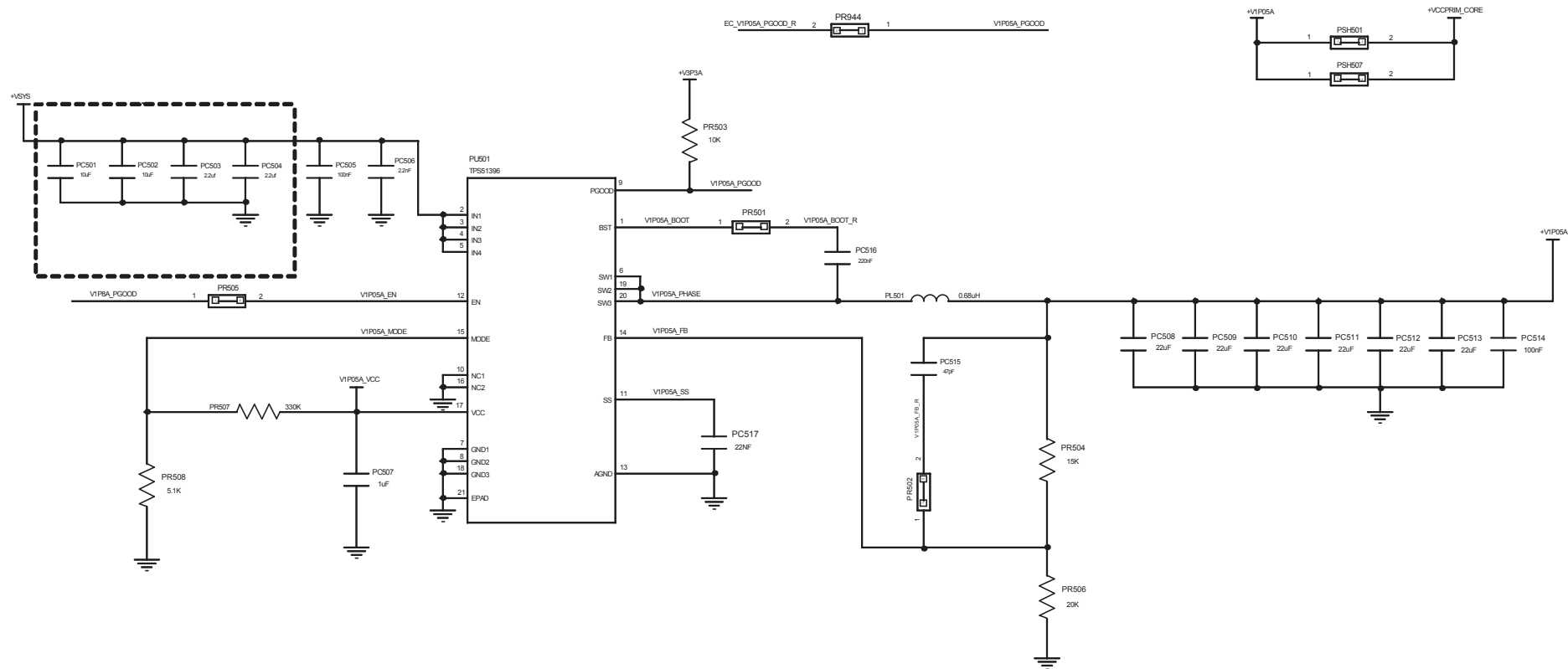


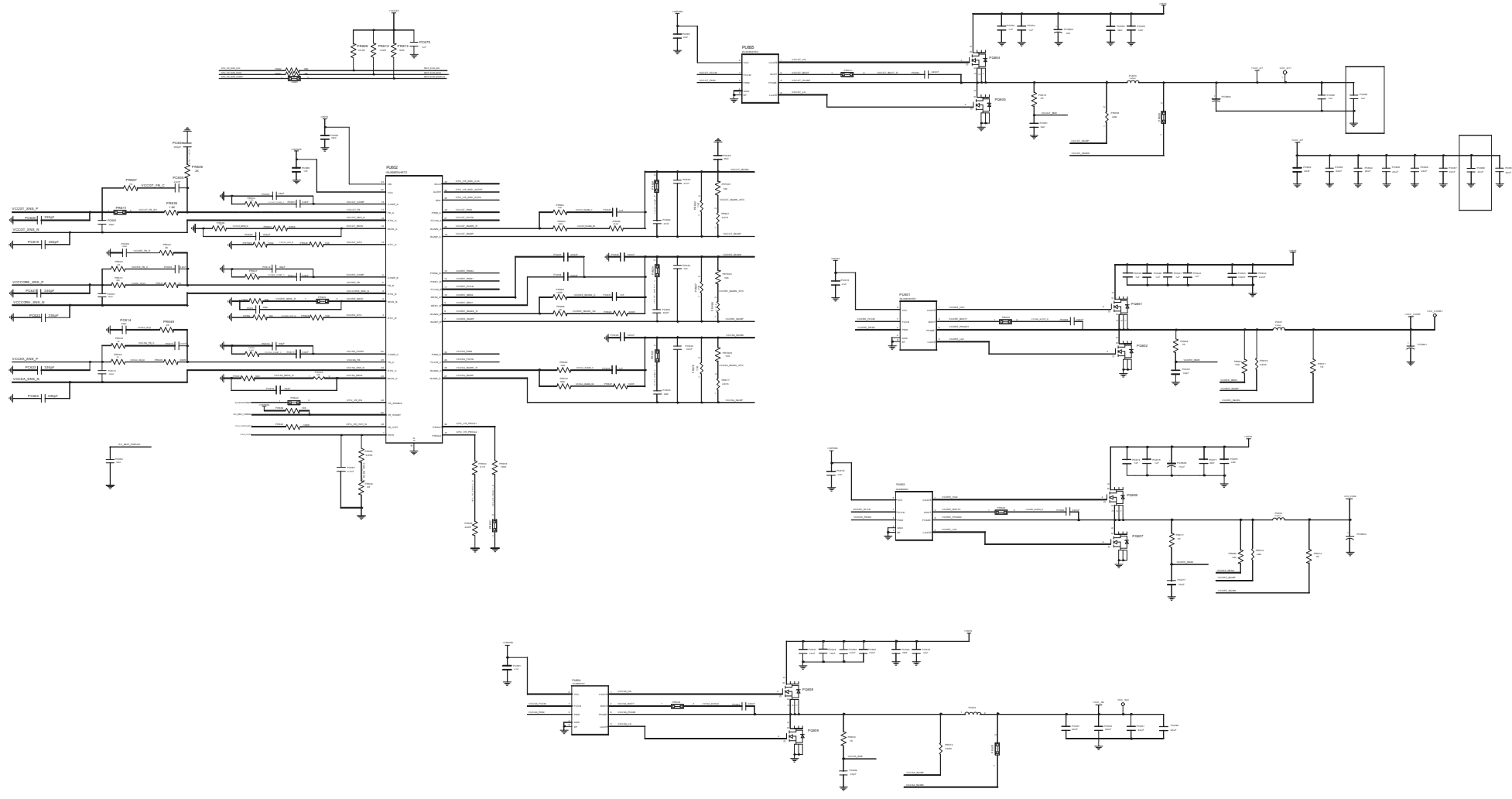


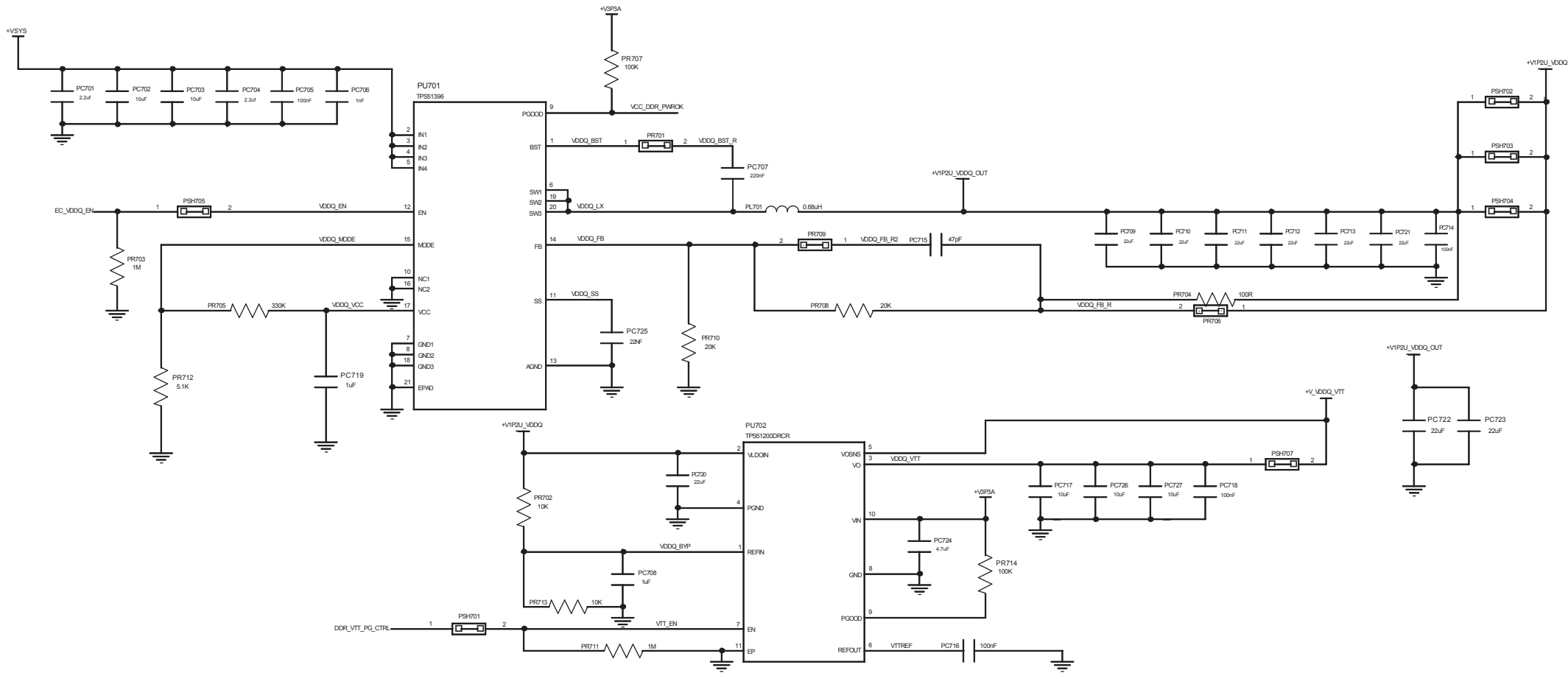


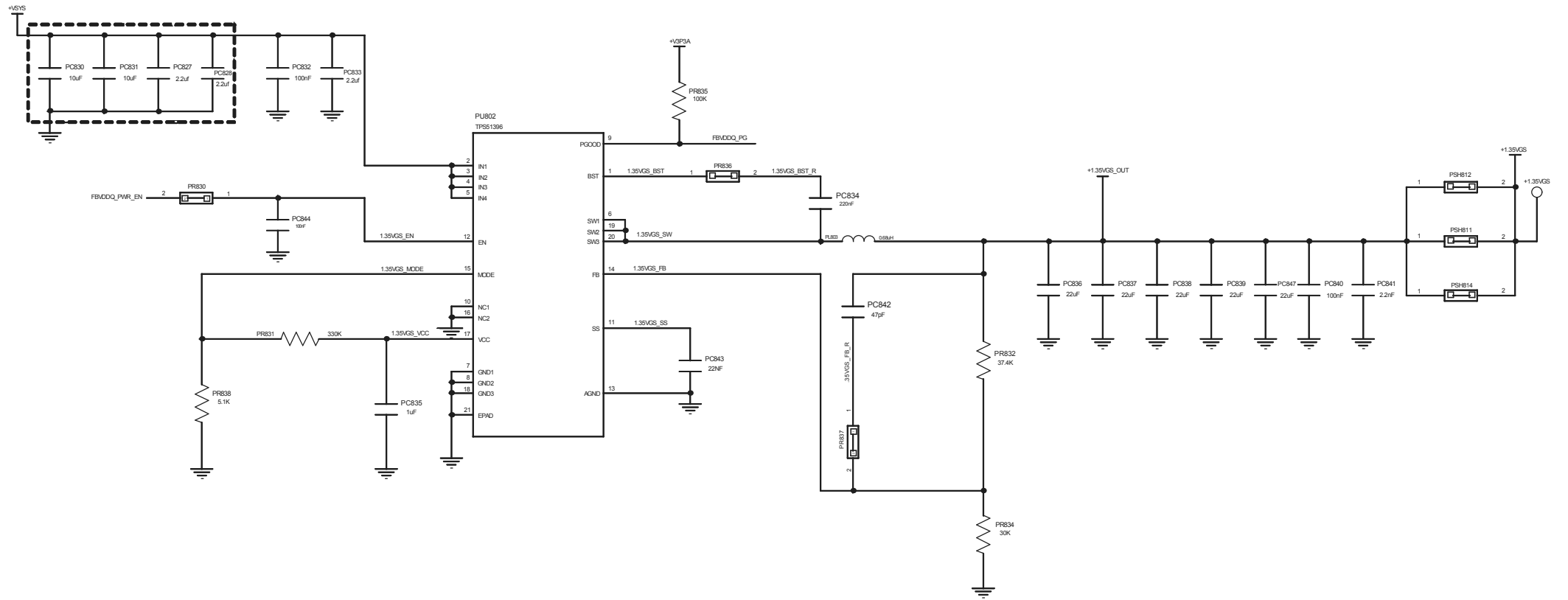


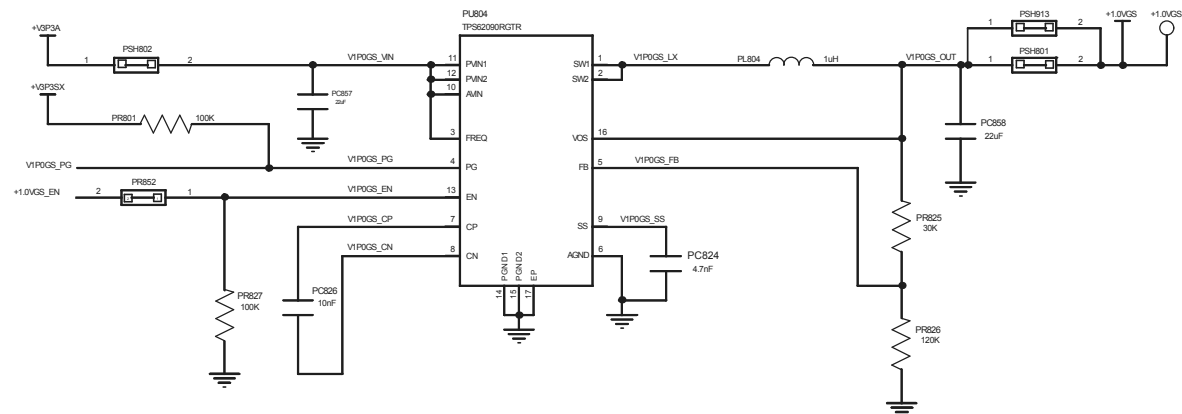


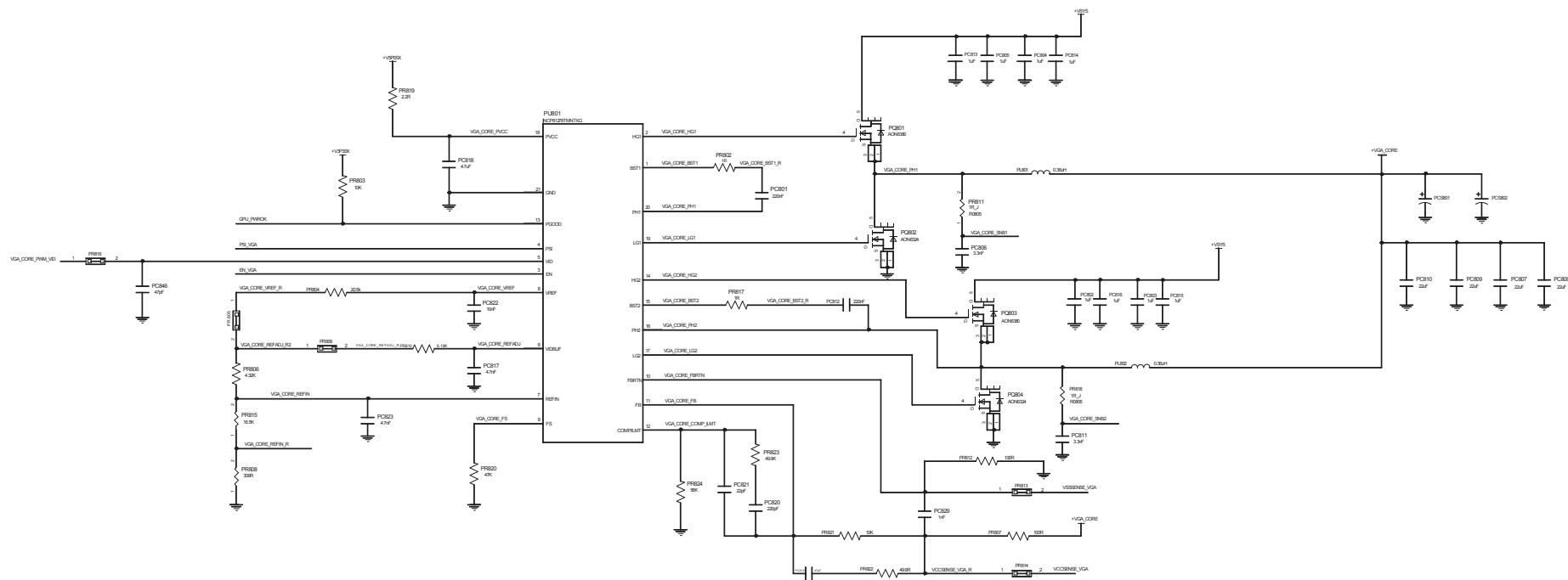




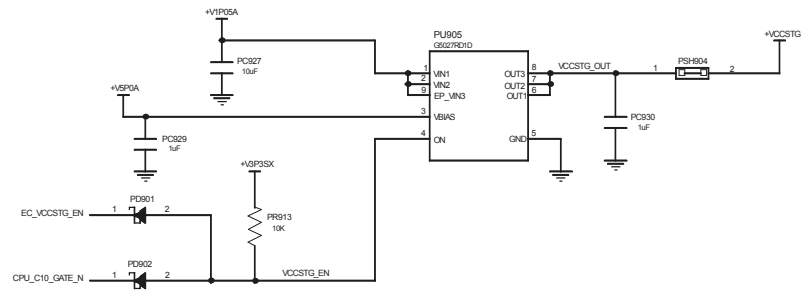




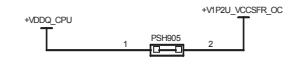




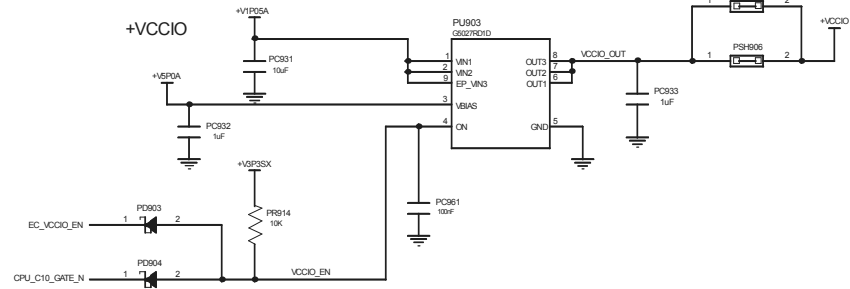
+VCCSTG



+V1P2U_VCCSFR_OC



+VCCIO



+VCCST

